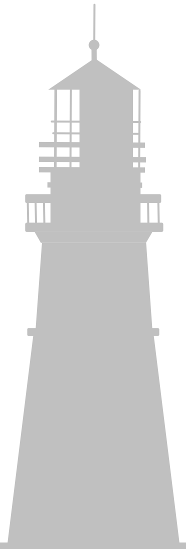

2006 Lithography Workshop

25th Anniversary

July 31 - August 4, 2006

Olde Charlottetown

Prince Edward Island

Canada

NOT FOR SALE

2006 Lithography Workshop

2006 LITHOGRAPHY WORKSHOP

July 31 – August 4, 2006
Prince Edward Island, Canada

www.ieeelitho.org

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Chairman's Message

Welcome to the 25th anniversary of the Lithography Workshop, which is being held from July 31 to August 4, 2006 at the Delta Prince Edward in Olde Charlottetown, Prince Edward Island, Canada, the birthplace of Canada. The Workshop held its first meeting in 1981 in Lake Placid, New York, site of the 1980 winter Olympics and site of the incredible U.S.A. hockey team victory over Russia. This will be the 17th Workshop held during the span of 25 years to promote the ever continuing evolution of lithography.

The Organizing Committee has arranged a technical and social program second to none and we trust you will avail yourself of all the sessions and functions they have planned.

The purpose of this Workshop is to share research advances in microlithography theory and practice, with relevance to current and long-term applications of microlithography technology. The Workshop format is intended to provide an atmosphere conducive to in-depth discussion of the invited papers presented in the technical sessions. This will be accomplished by giving each author 25 minutes for the presentation and questions. In order to promote free interchange, there will be no formal proceedings and no picture taking, recording, or references made to the Workshop presentations. The technical sessions have been scheduled for mornings and evenings so afternoons can be free to enjoy the beautiful surrounding areas.

Putting together a meeting such as this required the contributions of many people. We are especially thankful to the chairpersons who have put together the technical program. Each talk is invited and, therefore, each person on the technical program is being recognized for outstanding work in their field.

The Lithography Workshop cooperates with the IEEE Components, Packaging, and Manufacturing Technology Society and gratefully acknowledges the continuing support given by the following companies:

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Rohm and Hass Electr. Matls
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To preserve the Workshop atmosphere, attendance will be limited to 150. The Organizing Committee welcomes your comments and suggestions which can help better serve the lithography community. Those wishing to present significant results or appropriate rebuttal information should contact the program chairman.

John P. Reekstin
General Chairman

SCHEDULE OF EVENTS

TIME	EVENT	ROOM
Date: Monday, July 31, 2006		
08:00 - 23:00	Office	Stanley Room
17:00 - 22:00	Registration*	Lobby
18:00 - 22:00	Reception*	Prince Room
Date: Tuesday, August 1, 2006		
07:00 - 23:00	Office	Stanley Room
07:00 - 08:00	Attendee Breakfast	Edward Room
08:00 - 12:30	Technical Session	Prince Room
10:00 - 10:30	Morning Break	Prince Room
08:00 - 10:00	Spousal Breakfast	Consbrook Room
08:00 - 23:00	Spousal Hospitality	Consbrook Room
07:00 - 21:30	Technical Session	Prince Room
08:00 - 23:00	Attendee Hospitality Room	Island Room
18:00 - 19:00	Reception	Edward Room
Date: Wednesday, August 2, 2006		
07:00 - 23:00	Office	Stanley Room
07:00 - 08:00	Attendee Breakfast	Edward Room
08:00 - 12:30	Technical Session	Prince Room
10:00 - 10:30	Morning Break	Prince Room
08:00 - 10:00	Spousal Breakfast q	Consbrook Room
08:00 - 23:00	Spousal Hospitality	Consbrook Room
12:30 - 15:00	Committee Meeting & Lunch	Gulnare Room
07:00 - 21:30	Technical Session	Prince Room
08:00 - 23:00	Attendee Hospitality Room	Island Room
17:00 - 18:00	Reception	Island Room
Date: Thursday, August 3, 2006		
07:00 - 23:00	Office	Stanley Room
07:00 - 08:00	Attendee Breakfast	Edward Room
08:00 - 12:30	Technical Session	Prince Room
10:00 - 10:30	Morning Break	Prince Room
08:00 - 10:00	Spousal Breakfast	Consbrook Room
08:00 - 23:00	Spousal Hospitality	Consbrook Room
08:00 - 23:00	Attendee Hospitality Room	Island Room
17:00 - 18:00	Reception	Ballroom Foyer
18:00 - 21:00	Banquet & 25th Anniversary Celebration	Edward Room
Date: Friday, August 4, 2006		
06:00 - 17:00	Office	Stanley Room
07:00 - 08:00	Attendee Breakfast	Edward Room
08:00 - 17:00	Spousal Breakfast	Consbrook Room
08:00 - 12:30	Technical Session	Prince Room
10:00 - 10:30	Morning Break	Prince Room
12:00 - 13:30	Committee Member Only Wrap-Up Lunch	Valient Room

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* - Speakers please deliver USB drive or CD of slides to Ken Harrison at registration

2006 Lithography Workshop

Program Chairs

Prof. William Oldham and Prof. Andrew Neureuther
University of California Berkeley

Session Organizers

Optics	**John Bruning, Corning**
Optical Lithography	**Tim Brunner, IBM**
Maskless Lithography	**Nick Eib, LSI Logic** **Olav Solgaard, Stanford University**
EUV Lithography	**Alan Stivers, Intel** **Patrick Naulleau, Lawrence Berkeley Natl. Lab**
E-Beam Lithography	**Fabian Pease, Stanford University**
Imprint Lithography	**Grant Willson, University of Texas at Austin**
Resists and Beyond	**Juan de Pablo, University of Wisconsin-Madison** **Chris Ober, Cornell University**
Masks and Infrastructure	**Brian Grenon, Grenon Consulting**
DFM / Statistical Variation	**Luigi Capodieci, AMD** **Frank Schellenberg, Mentor Graphics** **Lars Liebmann, IBM** **Jim Wiley, Brion Technologies**
Beyond Chip Lithography	**Jeff Bokor, UC Berkeley**

Tuesday Morning, August 1, 2006
Technical Session 1
Prince Room
Session Chairs: Patrick Naulleau, Jim Wiley, Grant Willson

8:00 AM	**John Reekstin**		**Welcome**
8:10 AM	**Andy Neureuther** **William Oldham**		**Program Introduction** **Keynote Introduction**
8:20 AM	**Roxann Engelstad - Keynote Speaker**	**Univ. of Wisconsin**	**Thermomechanical Simulations to Facilitate the Development of Advanced Lithography**
	TECHNICAL SESSION START		
9:05 AM	**David Laidler**	**IMEC**	**Overlay Performance of an ASML Immersion Step and Scan Tool**
9:30 AM	**Alan Stivers**	**Intel**	**EUVL Transition to High Volume Manufacturing**
9:55 AM	**BREAK (30 min)**		
10:25 AM	**Paul Nealey**	**Univ. of Wisconsin**	**Enhanced Information Transfer in the Lithographic Process Using Block Copolymer Resists**
10:50 AM	**Andres Torres**	**Mentor Graphics**	**Litho Friendly Design as the Precursor to Improved Electrical Analysis**
11:15 AM	**Jim Ellenson**	**Hewlett Packard**	**Imprint Lithography:Getting to the Next Level**
11:40 AM	**Larry Zurbrick**	**KLA-Tencor**	**Reticle Inspection for 45 nm and Below, Challenges Redux or Anew?**
12:05 PM	**Bert Jan Kampherbeek**	**MAPPER Lithography**	**High Throughput Maskless Lithography**
12:30 PM	**END SESSION**		

Thermomechanical Simulations to Facilitate the Development of Advanced Lithography

Roxann L. Engelstad
Computational Mechanics Center, University of Wisconsin
1513 University Ave.
Madison, WI 53706

Modeling and simulation of advanced lithographic processes and components is necessary if the semiconductor industry is to meet the stringent requirements of the lower lithographic nodes in a timely manner. Design and optimization tools for optical systems, imaging performance, optical proximity corrections, etc., are continually being utilized for current and future technologies. However, *thermomechanical simulations* are also being recognized as a means to reduce the development time of new processes and components, including the fabrication and use of advanced masks. This presentation describes the details of the computational fluid dynamics (CFD) modeling which identifies the fluid management issues associated with immersion lithography (Fig. 1). For extreme ultraviolet lithography (EUVL), the latest results from the finite element (FE) models generated to predict the response of EUVL reticles during electrostatic chucking will be presented (Fig. 2). Additional simulations illustrating fluid / structure interaction in nanoimprint lithography will be shown. In essence, the FE and CFD simulations demonstrate the viability of using thermomechanical models to facilitate the timely development of advanced lithography technologies.

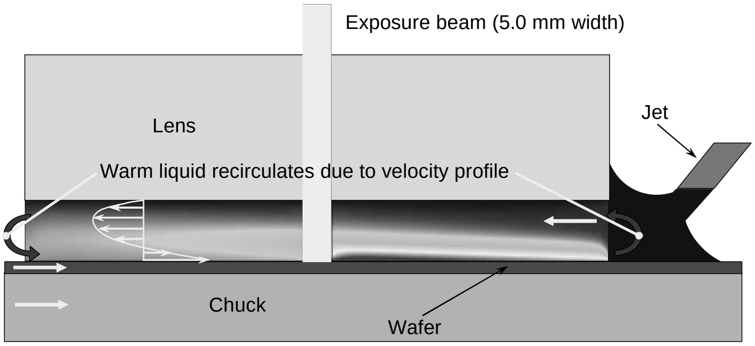


Fig. 1. Flow profile and thermal distribution for opposing flow during immersion lithography exposure scanning as predicted by CFD simulations.

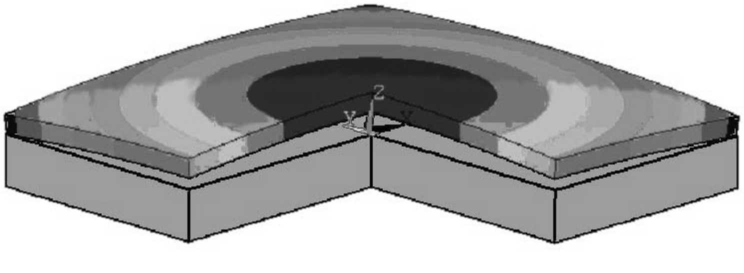


Fig. 2. Cut-away view of the FE model simulating the electrostatic chucking of an EUVL reticle.

Overlay Performance of an ASML Immersion Step and Scan Tool

David Laidler and Shaunee Cheng
IMEC, Kapeldreef 75, B-3001 Leuven, Belgium.

Abstract

In order for immersion lithography to be manufacturable, the same overlay performance must be achieved as for state of the art dry step and scan tools. Not only must it be able to demonstrate this performance, it must be able to maintain this performance consistently over time. In this paper we evaluate the overlay performance of an ASML XT:1250Di immersion step and scan tool, highlighting the issues observed during the long term evaluation, the achievable overlay performance and compare this performance to an equivalent dry tool. The paper will look at both grid and intrafield performance by use of appropriate sample plans, looking at immersion specific fingerprints and how they can be optimised. Performance data will be shown for both single machine and matched machine overlay, where the system matched to is a state of the art dry tool. New techniques for further improving the overlay performance will also be presented and the importance of timing and delay issues caused by an interfaced track will be discussed.

Keywords: Overlay, Immersion, Step and Scan, ASML, XT:1250Di, Grid, Intrafield.

EUVL Transition to High Volume Manufacturing

Alan R. Stivers* and Melissa Shell**
Intel Corporation
*SC1-03, 3065 Bowers Ave., Santa Clara, CA 95054
**RA3-252, 2501 NW 229th Ave., Hillsboro, OR 97124

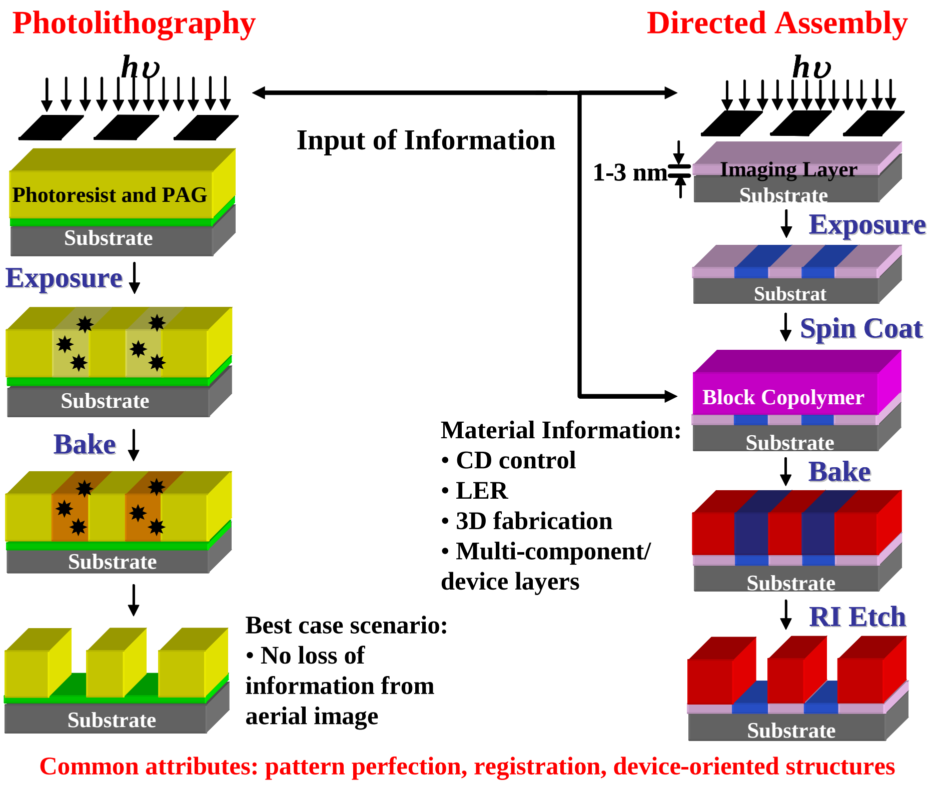
Semiconductor chip manufacturers need capable lithography solutions on time to benefit from the economies of semiconductor scaling. Lithography processes and tools are intimately connected to the feature size and therefore must be upgraded with each new technology node. More often than not this is done with an increase in numerical aperture or other resolution enhancement. This has its limits, so the industry has historically needed to take advantage of the extendibility offered by wavelength scaling.

This presentation will discuss the process of implementation of a new lithography wavelength, with emphasis on EUV. We will cover how requirements are defined and how gaps are assessed. We will also discuss the role of suppliers, consortia, and end users in facilitating the smooth transition from research to development to production. We will touch on both technical risks and business risks. Just as suppliers need to learn how to build the necessary tooling, users need to learn how to integrate the technology with the rest of the fabrication process. Given the unique risks associated with changing from 193nm lithography to EUV, it is expected that the transition through development to prepare for high volume manufacturing could take one technology generation. Further, this transition will not begin in earnest until the pre-production exposure tools are on the factory floor running wafers. True adoption of EUV lithography will no occur until two of three figures of merit are achieved: faster, better, cheaper.

Enhanced Information Transfer in the Lithographic Process Using Block Copolymer Resists

Paul F. Nealey
Department of Chemical and Biological Engineering
University of Wisconsin
Madison 53706

In the photolithographic process, information encoded in the aerial image of the exposure tool is transferred to the photoresist through a series of processing steps that culminate in the creation of patterned three-dimensional features. As feature dimensions shrink below 30 to 50 nm, however, the fidelity of the transferred information using current resists may not meet manufacturing requirements, particularly with respect to control over the size and shape of the patterned features (e.g. critical dimension control and line edge roughness). We are investigating the integration of self-assembling block copolymers into the lithographic process such that the materials themselves contribute valuable information towards the desired ends. At the same time we retain essential process attributes such as pattern perfection, registration and the ability to pattern non-regular device-oriented structures. Our approach is to lithographically define chemically patterned surfaces to direct the assembly of overlying films of block copolymers and block copolymer/homopolymer blends (see Figure below). We demonstrate that through tailored interfacial interactions, it is possible to pattern many of the essential isolated and dense geometries used in device design with precise (sub 1 nm) control over the dimensions and shapes of nanoscale patterned resist features. We also demonstrate that this technology platform can be used to fabricate addressable complex three-dimensional structures or multiple device layers in a single lithographic step. Strategies will be discussed to implement this technology for improved performance and reduced cost.



Litho Friendly Design as the Precursor to Improved Electrical Analysis

Torres, Andres
Mentor Graphics

The concept of Litho Friendly Design, is based on the intelligent exchange of process variability information between fabrication facilities and design centers. The process information is used to determine the pattern sensitivity that a given layout exhibits when subject to pre-defined set of process variations. Because pattern sensitivity is highly dependent on layout configuration, the designer can examine different sensitivity trade-offs between multiple layout configurations.

While it is possible to minimize pattern sensitivity by selecting very homogenous structures, the sensitivity cannot be completely eliminated because such sensitivity highly depends on the process being used. Traditionally this pattern sensitivity was embedded in the statistical calibration of SPICE models, and the availability of fast, slow and mix mode models. However, with diminishing features sizes and exposure tools remaining at 193nm, along with etch and CMP effects, the contribution of configurational neighborhoods make such calibration extremely difficult without having to consider relatively large margins.

It is only until recently that the ability to deterministically create the transformations from layout to process images is finding its way to designer's desktops which means, that this capability can be used not only to determine layout topology violations, but explicitly use such information to enhance device and interconnect extraction.

This paper highlights the types of electrical analyses that can be implemented with very limited modifications to existing design flows.

Imprint Lithography: Getting to the Next Level

James E. Ellenson; Ken Kramer; Tim S. Hostetler; Laura King; William M. Tong
Hewlett-Packard Company
1000 NE Circle Blvd.
Corvallis, OR

The scope of the presentation is examination of novel nanoimprint applications, specifically the efforts being done in Quantum Science Research at HP Labs as well as photonic crystal waveguide work at Corvallis' Technology Development Organization. We will review several nanoimprint techniques. We looked at the opportunities imprint lithography has compared to traditional optical lithography. In addition, we will review important aspects of nanoimprint and what technical challenges and key areas need to be resolved in the next five years to enable this technology to become commercially viable.

Reticle Inspection for 45 nm and Below, Challenges Redux or Anew?

Larry Zurbrick
KLA-Tencor Corporation
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San Jose, CA 95134

Reticle inspection requirements beyond 45 nm half pitch present a challenging set of tradeoffs from both a technical and business perspective.

The ITRS Roadmap only states potential lithography solutions for future nodes that the industry views as the most likely technical scenarios without regard to infrastructure investment associated with each potential solution. Currently the ITRS Roadmap states the most likely lithography candidates after 193 nm (193i) immersion are EUV, Imprint, and ML2 (Mask-Less Lithography). Inspection system requirements associated with each potential post-193i lithography solution do not comprise a common set of inspection system requirements either from a hardware implementation or defect detection viewpoint.

The choice of lithography strategy determines reticle inspection requirements and for two potential lithography strategies in the sub-45 nm regime, the term “reticle” is inappropriate since pattern transfer is accomplished by a template or by a beam of electrons. Even as such, pattern fidelity will need to be verified by some inspection tool that is different from what exists in the market today. EUV reticle inspection may have the closest resemblance to current reticle inspection techniques, but has several unique inspection requirements associated with its structural composition and handling requirements. Recent discussions in the industry have centered on the use of Double Patterning (DP) with 193i scanners and suggest that a potential “maskmakers vacation” may just be around the corner. DP reticle inspection requirements suggest that the “vacation” will be short.

High Throughput Maskless Lithography

B.J. Kampherbeek
MAPPER Lithography
Computerlaan 15
2628 XK, Delft, The Netherlands

MAPPER has been working for some time on its technology demonstrator: A machine that is capable of exposing a wafer with 110 electron beams in parallel. The target specs are based on the 45 nm half pitch technology node.

The MAPPER technology combines massively-parallel electron-beam writing with high speed optical data transport used in the telecommunication industry. The electron optics generates 13,000 electron beams that are focused on the wafer by electrostatic lens arrays. Each beam has its own optical column to avoid a central cross-over, see figure 1. This secures high throughput (> 10 wafers per hour) at high resolution (< 45 nm). The 13,000 e-beams are generated by splitting up a single electron beam that originates from a single electron source. The e-beams are arranged in such a way that they form a rectangular slit with a width of 26 mm, the same width of a field in an optical stepper. During exposure the e-beams are deflected over 2 µm perpendicular to the wafer stage movement. This means that with one scan of the wafer a full field of 26 mm x 33 mm can be exposed. During the simultaneous scanning of the wafer and deflection of the electron beams the beams are switched on and off by 13,000 light signals, one for each e-beam. The light beams are generated in a data system that contains the chip patterns in a bitmap format. This bitmap is divided over 13,000 data channels and streamed to the e-beams at 1-10 GHz.

In the presentation the results of the technology demonstrator will be presented.

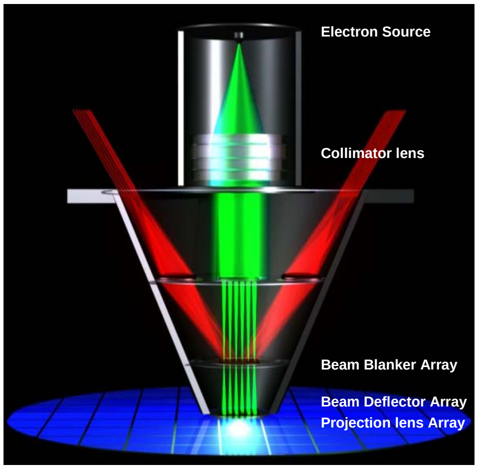


Figure 1. Schematic outline of MAPPER's e-beam column

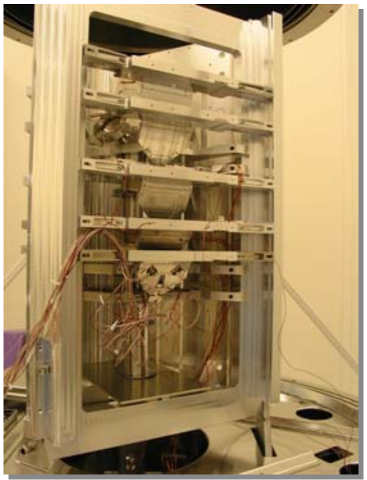


Figure 2. E-beam column for technology demonstrator

Tuesday Evening, August 1, 2006
Technical Session 2
Prince Room
Session Chairs: Juan de Pablo, Luigi Capodieci

7:15 PM	**ANNOUNCEMENTS**		
7:20 PM	**Griff Resor**	**Resor Associates**	**Flat Panel Lithography**
7:45 PM	**Tatsuhiko Higashiki**	**Toshiba**	**Status and Future of Immersion Lithography**
8:10 PM	**Mark Mason**	**Texas Instruments**	**Litho-Aware Model-Based Design Rule Checking for 45nm Node**
8:35 PM	**Chris Ober**	**Cornell University**	**Molecular Glass Resists: Do We Need Polymers Anymore?**
9:00 PM	**Grant Willson**	**UT, Austin**	**Imprint Lithography for Dual Damascene**
9:25 PM	**END SESSION**		

Flat Panel Display Lithography

Griff Resor
Resor Associates
629 Massachussetts Ave, #200
Boxborough, MA 01719

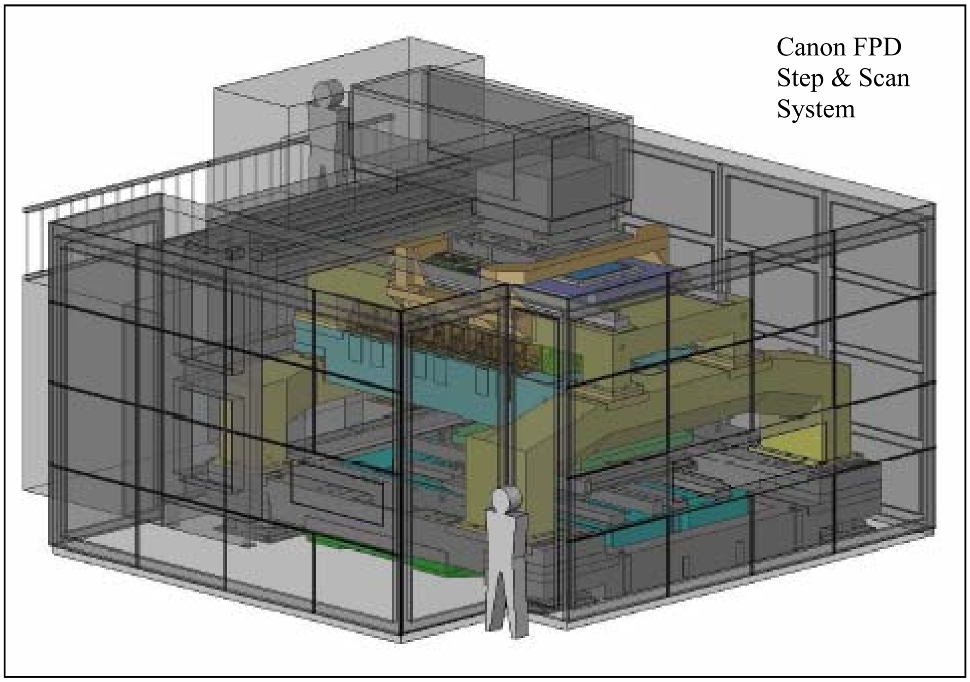
The TV that looks like a picture and hangs on the wall has arrived. Plasma TV and Liquid Crystal TV [LCD-TV] technologies are competing for market share. At the same time TV is moving from analog to digital, and the image is doubling its width as the world moves to HDTV. A review of these trends will be provided.

The competition in TV markets is driving internal changes in Liquid Crystal TV's. Layers, structures and patterns that improve LCD-TV performance are being added. The basic internal structures and recent changes will be briefly explained. These added layers, structures, and patterns impact Flat Panel Display Lithography. The basic lithography requirements for Liquid Crystal Flat Panel Displays will be described.

Three kinds of lithography tools are used to manufacture LCD-TV's today. Giant step and scan systems from Canon and Nikon print the tightest tolerance layers. Step and Repeat Proximity printers are used for the remaining layers. Smaller Step and Repeat projection systems are used to print mobile display circuit patterns.

The basic operation of the Canon and Nikon step and scan lithography machines will be described. Drawings and pictures will be used to describe the main internal subsystems. While both machines are 1X projection systems, the Canon and Nikon machines differ significantly in their optical design. This will be explained. A throughput example will be presented.

Masks used in these machines will be briefly described. A related paper by Chris Progler of Photronics follows. Chris will provide added detail about FPD masks.



Status and Future of Immersion Lithography

Tatsuhiko Higashiki[1)], Shinichi Ito[1)], Yuuki Ishii[2)], Soichi Owa[2)]

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[2)] Nikon Corp., Precision Equipment Company, Development Headquarters
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ABSTRACT

Immersion optical lithography for mass production is close to becoming reality. Using current 193 nm ArF light sources, immersion exposure technology allows dramatic increases in lens numerical aperture (NA), extending the life of ArF lithography technology. Production lithography from 65 nm to 45 nm half pitch (hp) will be realized by ArF immersion lithography.

Immersion-specific technical issues, such as defectivity, overlay accuracy, and focus variation, must be resolved to realize immersion lithography. Nikon developed the Engineering Evaluation Tool (EET, NA=0.85) at the end of 2004 to address fundamental immersion issues, and the EET was installed at Toshiba. Using this tool, the mechanism of watermark defect formation was identified[1)], enabling the elimination of watermark defects through process optimization. Recently, the evaluation of an advanced Nikon immersion tool, S609B (NA=1.07) has begun. This paper will focus on recent data on fundamental immersion issues, and the newest data from S609B.

In 45 nm hp lithography, the 3-D structure of the mask and resist processing details require special consideration to avoid polarization issues. Furthermore, 32 nm hp lithography by double patterning requires higher overlay accuracy. These issues and others make future lithography more difficult than previous generations. This paper will also provide some insight into technologies for future lithography.

References

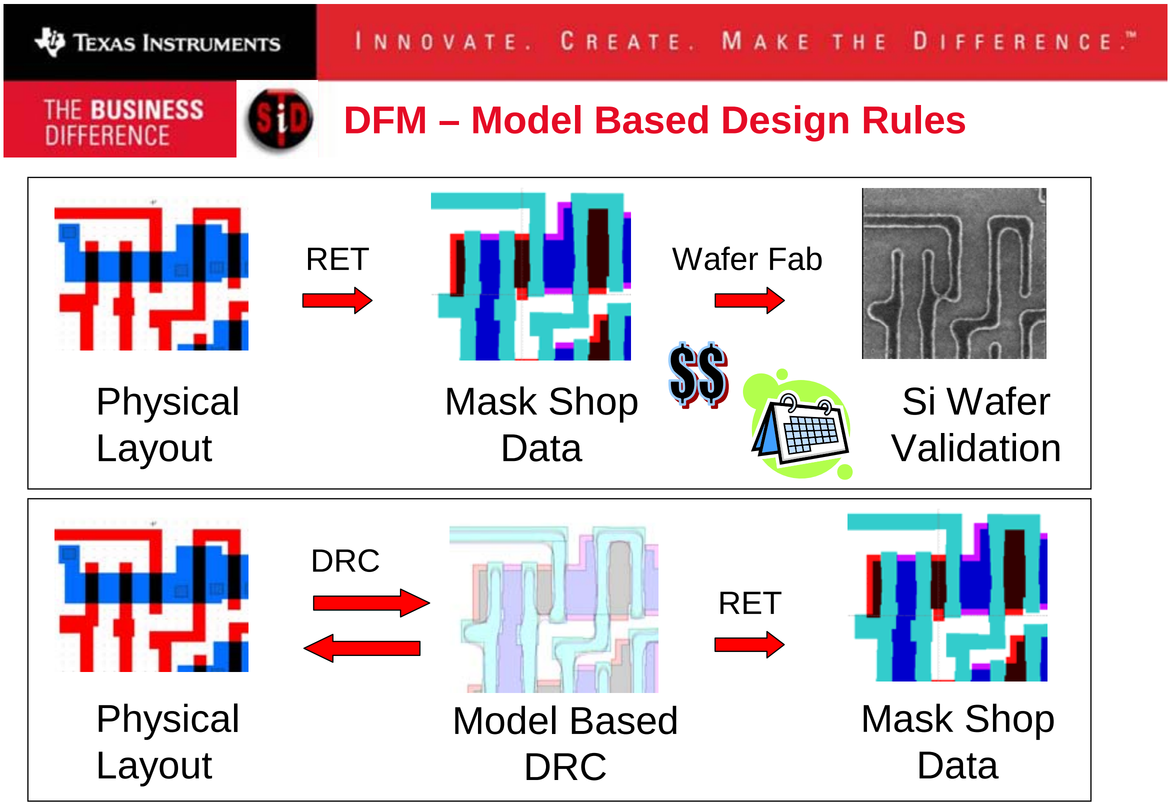
1) Daisuke Kawamura, et al, “Influence of the Watermark in Immersion Lithography Process”, proc. of SPIE, 5753-95, 2005

Litho-Aware Model-Based Design Rule Checking for 45nm Node

Mark Mason, Lewis Flanagin, Mark Terry, Shane Best, Carl Vickery, Graham Barr
Texas Instruments, Incorporated
P.O. Box 650311, Mail Station 366, Dallas, Texas 75265

At the last IEEE Lithography meeting in 2004, the author examined Design for Manufacturability (DFM) considerations and lessons learned from the successful implementation of various RET strategies at the 90 nm node at Texas Instruments. At that time, the need for a model based approach for Design Rule checking was predicted. Since that time, additional data at the 65 nm and 45 nm logic nodes has supported that conclusion.

In this discussion, we update the status of model-based design rule checks (MBDRCs) at Texas Instruments. Recognizing the current EDA industry DFM trend to push process information up into the design flow, and using the 45 nm logic node development as a backdrop, we detail the need for such checks, issues with their implementation, and implications of their use and deployment into the design community.


Texas Instruments
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THE BUSINESS DIFFERENCE
DFM – Model Based Design Rules

Figure 1: A traditional RET flow, with design rules as the collection point for process information as compared to a model based flow, where complicated lithographic interactions can be anticipated and avoided.

Molecular Glass Resists: Do We Need Polymers Anymore?

Christopher K. Ober, Anuja de Silva, Drew Forman, Xavier Andre, J. K. Lee, Nelson Felix
Materials Science & Engineering
Cornell University
310 Bard Hall
Ithaca, NY 14853

Molecular glasses are a family of glass forming organic molecules that only recently have been investigated as high-resolution photoresists. Design concepts come largely from the organic electronics community where these materials have been investigated as new, glass forming semiconductors. As studied these materials are of limited molecular dimension (molecular weights less than 100 g/mol and molecular size on the order of 1 nm). Their complex shape helps to inhibit crystallization and they can easily be made for solubility in aqueous base or a wide range of solvents. In contrast, one of the challenges of working with today's polymeric photoresists is the fact that even the small size of these polymers approaches that of the target features of next generation lithography.

By using molecular glasses, the effective pixel size of the resist is reduced to ~1 nm. This presentation describes recent developments in the synthesis and lithographic processing of these new materials. Several families of materials will be described: (i) molecular glasses based on branched structures and (ii) ring systems capable of very high resolution imaging. Both families have been shown to be capable of forming images smaller than 50 nm using both e-beam and deep UV lithography. The effect of molecular structure, resist composition and photoacid generator on resolution and line edge roughness will be discussed.

Acknowledgement: The authors would like to thank Intel, International Sematech and the Semiconductor Research Corporation for funding different aspects of the reported work. We thank Lawrence Berkeley National Laboratories for EUV exposures.

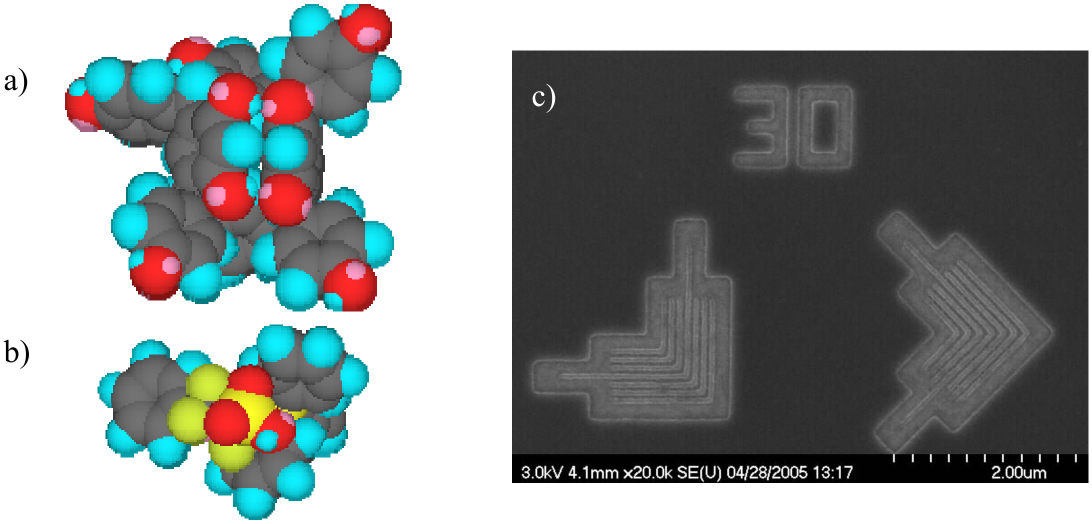

Figure: Example of molecular glass photoresist – this photoresist consists of (a) a calix-resorcinarene with (b) a non-PFOS photoacid generator. (c) The t-BOC protected version of (a) is capable of sub-50 nm pattern formation using EUV exposures.

Imprint Lithography for Dual Damascene

Grant Willson

The Department of Chemical Engineering, The University of Texas, Austin, Texas

"Back End of Line" (BEOL) processes are those that produce the interconnect wiring in microelectronic devices. This circuitry is required to link transistors and circuit elements to one another, to bring signal and power to the devices and to allow them to communicate with the outside world. A modern integrated circuit device may require as many as ten levels of interconnected wiring to make all of these connections. The trench first, dual damascene process used to generate these copper interconnects requires over 100 processing steps, many of which are very challenging. BEOL processing using Step and Flash Imprint Lithography (SFIL) can dramatically reduce the number of processing steps required to fabricate these interconnect structures because a single SFIL imprint step can generate a plating template for both a via and a wire simultaneously. We are pursuing two paths to exploit this great saving in the number of steps in the process. The first involves patterning a sacrificial, photosensitive etch barrier material by imprint lithography and then transferring that relief structure into a standard CVD dielectric stack by reactive ion etching. In this way, many lithography, steps, hard-masking materials and pattern transfer processes are eliminated. The second SFIL implementation involves directly patterning a photosensitive dielectric material instead of a sacrificial resist material. In this way over 100 process steps can be avoided in production of just 8 metal layers, but a new insulator material is introduced into the device which demands consideration of both function and reliability concerns. This presentation will report progress on the development of new materials for both of the SFIL-BEOL processes and describe their integration into the wafer process flow at the SEMATECH Advanced Technical Development Facility.

Wednesday Morning, August 2, 2006
Technical Session 3
Prince Room
Session Chairs: Olav Solgaard, Alan Stivers

8:00 AM	**ANNOUNCEMENTS**		
8:05 AM	**Tor Sandstrom**	**Micronic Laser Systems**	**SLM Lithography: Towards Real-time OPC and Inverse Rasterisation**
8:30 AM	**Joseph Pankert**	**Phillips Extreme UV**	**EUV Sources: The pain of getting the right photons**
8:55 AM	**Rick Dill**	**Hitachi GST**	**CMP Assisted Patterning**
9:20 AM	**Juan Schneider**	**Nanometrix**	**A Novel Method for Thin Film Production**
9:45 AM	**BREAK (30 min)**		
10:15 AM	**Dan Sanders**	**IBM**	**Oil or Water: What's the Difference for 193 nm Immersion Lithography?**
10:40 AM	**John Burnett**	**NIST**	**High-Index DUV Optical Materials**
11:05 AM	**Jun Ye**	**Brion Technologies**	**Applied Image Computing for Computational Lithography**
11:30 AM	**Ralph Dammel**	**AZ**	**Ultrathin Resists for Immersion and EUV: Reflectivity Control, Integration and Fundamental Issues**
11:55 AM	**Prof. Bruce Smith**	**RIT**	**Lithography using the Evanescent Field - Is it Worth the Frustration?**
12:20 PM	**END SESSION**		

SLM Lithography:
Towards Real-time OPC and Inverse Rasterisation

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Recently model-based OPC has become all but a necessity for lithography. The pattern is processed in the vector domain prior to being sent to the mask writer. There are high penalties in pre-processing time and data file size.. An optical SLM-based maskwriter has similar proximity properties as the wafer scanner, but in scale 4X. Ideally the maskwriter data should be OPC processed once more, increasing turn-around time, pre-processing cost and data file size even more. But can the second processing step not be simplified and run concurrently with the optical writing? And if such a system can be designed for masks, cannot it not be used to write high-fidelity patterns directly on silicon as well?

In order to allow real-time OPC we simplify the problem in a number of ways: First, we introduce an illumination distribution and a matching pupil filter that gives neutral printing properties, but with a "pre-emphasis" of high spatial frequencies. Secondly we match the pixel grid to fit to the imaging kernel. Then the kernel is culled to reduce the number of elements. With the optical filtering a straight rasterization makes the printed pattern a reasonable approximation to the data, and with the simplified kernel a single one-step adjustment of each boundary mirror is computed and applied. The result is an improvement in resolution and fidelity for general 2D patterns with a modest cost in real-time processing.

Described so far is only edge adjustment for better CD control, but with no improvement of process latitude. Recently so called inverse lithography has become commercially available from other sources. The mask pattern goes through a non-linear optimization and both edge positions and process latitude can be included in the merit function. Ongoing work shows that similar optimization can be done with the tilt of the mirrors, which provides more correctivve power than a mask can give. The optical filters described above and the reduced kernel makes the computation efficient. The "dumb" rasterization makes a good starting approximation and few iterations are needed for convergence. Compared to edge-only correction the full non-linear optimization promises better resolution, better edge sharpness, and above all better depth of focus.

The impetus of the work has been to design a better maskwriter, but it is equally applicable to maskless wafer lithography. The maskless writer would need to be set up with the proper optical filtering, but would then write any pattern *a vista*, i.e. immediately without preprocessing.

EUV Sources: The pain of getting the right photons

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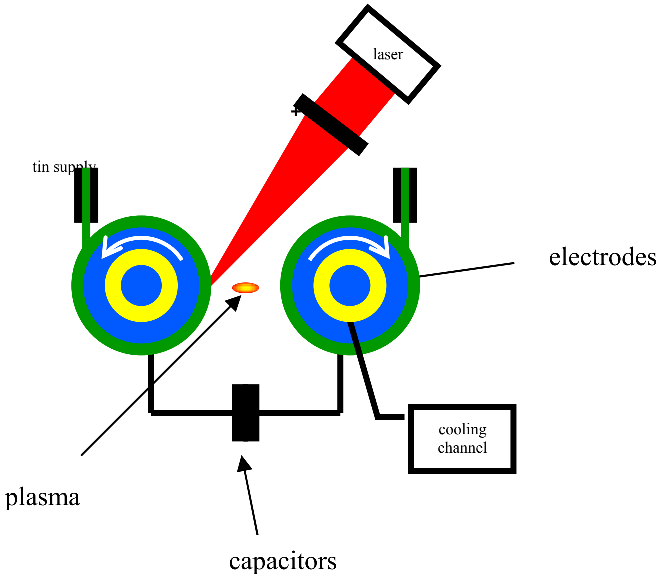
EUV sources have been a very popular subject ever since short wavelengths have been considered for lithography. Many academic groups and companies have engaged in research and development of plasma sources. The reason is that it requires studying a wealth fascinating problems of plasma and materials physics. As a result, the community has come forward with many interesting ideas of how to generate EUV with the right wavelength and how to integrate the system into an EUV scanner.

The most promising and most advanced concept is a Sn based gas discharge lamp with rotating electrodes. The concept combines a number of important features: Sn is the fuel with highest efficiency as it radiates in the right wavelength range, rotating electrodes allow for scaling to excessively high power values. Moreover, a recovery mechanism of the electrode surface allows for virtually unlimited electrode lifetime. A sketch of the lamp is shown in below figure.

The second big issue of EUV sources is collector integration and collector lifetime. This subject is a particular challenge since a lot of Sn vapor will be released to the vacuum system. The collector is the first optical element down the optical train and receives an excessive amount of heat load, but also Sn vapor and fast Sn ions. Collector protection mechanisms will be discussed, along with cleaning schemes with which contaminated collectors can recover their original reflectivity.

Finally results on integration of the source into scanners will be discussed.



CMP Assisted Patterning

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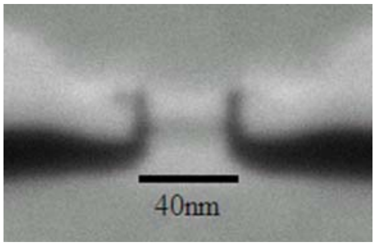
Abstract

CMP Assisted Patterning is a new process used for building magnetic electron device structures, in particular magnetic recording heads for disk drives, an industry where microfabrication technologies have been used for less than 30 years. A decade ago, the minimum printed feature was about 3 microns, I-line lithography was used, and the topography due to structures built on the wafer was largely ignored. The introduction of CMP planarization along with the transition from inductive read sensing to magneto-resistive elements, followed by spin-valve sensors, and moving today into magnetic tunneling sensors , has allowed rapid convergence of feature size in recording heads to that of microcircuits and recording density increases of up to 100% per year.

The purpose for lithography isn't just about building beautiful and tiny structures out of photoresist. It is about using those structures to build things useful to mankind. Traditionally the thin-film materials used in building recording heads are difficult to pattern using conventional RIE so that ion milling is the commonly used etching process and the patterning some metal films is done with bi-layer resists and an overhanging structure, i.e. the stencil lift-off process now long abandoned in microelectronics. The lift-off process gets exceedingly difficult as read sensor dimensions creep below 100 nm. This paper will present a novel approach to self-aligned patterning of difficult to etch films using a CMP (Chemical Mechanical Polishing) to assist in the process. Examples will be shown that demonstrate that this patterning approach can work to below 20 nm.



TEM Image of 40 nm experimental read sensor

A Novel Method for Thin Film Production

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A novel method was invented for coating rigid and flexible surfaces with films. The process, named Linear Coating, runs at high linear speed with uniform quality. A film can be made from fine structures like nano or micro spheres, monomers or polymers. In this case, the 2D assembly is a monolayer. When the film is made from organic material in such a way that molecules are intermingled in a non preferential direction, we name it thin film, for micron thicknesses and ultra thin film if we are in the 10 nm range. This versatile process offers a wide range of possibilities, among them the elimination of edge bead and potentially increase five times the number of wafers produced with same resist quantity. Therefore, this coating method is a real alternative for lithography and mask production as well as a concrete alternative for the industrialization of monolayer coatings.

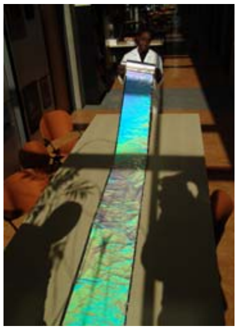

Figure 1

Monolayers made with fine powders, namely TiO_2, SiO_2, nano diamonds and proteins were prepared. Figure 1 shows a polycrystalline monolayer of one micron diameter SiO_2 beads with pearlescent effects. The SiO_2 monolayers were also used as templates for gold patterning wafers. E-beam direct writing on 8 nm PMMA ultra-thin films, and photolithography on 30 nm UV-1400 DUV resist thin films are also presented. Figure 2 shows an example of 30 nm DUV resist with patterns obtained after UV exposure and development.

Monolayers are built by sliding elements on the surface of a liquid until they meet the monolayer formation line. The natural flatness and fluidity of the liquid surface is used, and its flow drives and packs the elements one against the other in an orderly and continuous way. At the same packing rate, the monolayer is transferred onto a substrate. A self-calibrating dynamic and continuous equilibrium is our proprietary feedback loop. The rate of production exceeds one square meter per minute, which means typically, for a molecular scale element, that several billion elements per second are integrated in the monolayer matrix.

So far, monolayers and multilayers of many kinds and types of materials have been produced and displayed. Polymer film thicknesses can be tailored to different values starting from 1 nm and up with sub nanometre roughness. Bulky micron thick polymer films can be engineered as well with surface roughness below 1 nm. Multilayers made from the superposition of several ultra thin films are also produced.

The user friendly control of thinness, uniformity, molecular orientation, and organization of matter with reliability, high throughput and low costs are what best characterizes the Linear Coating process. These qualities match the increasing demand for leading edge nanotech based devices such as optical components, photonics, flat panel displays, flexible electronics, micro- and nano-electronics, MEMS and nanolithography.

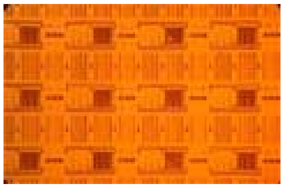

Figure 2

Oil or Water: What’s the Difference for 193 nm Immersion Lithography?

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High index immersion lithography has emerged as a potential candidate to extend immersion lithography beyond the 45 nm node and delay the need to implement next generation lithographic techniques such as EUV lithography. High index immersion lithography simply employs a higher refractive index fluid and lens material to gain additional benefits beyond that afforded by the initial move to water immersion lithography. Over the last two years, a number of organic fluids have emerged as the most promising high index fluids, displaying higher refractive index and higher transparency than the best water-based high index fluids. We have previously demonstrated sub-30 nm half-pitch imaging using interferometric lithography with an organic high index fluid. However, the difficulty of developing a suitably high refractive index lens material has raised the possibility of a high index fluid-only node (NA = 1.45-1.5). Clearly, significant lithographic and/or process benefits would be required to justify such a node and, therefore, understanding the potential benefits of moving to an organic immersion fluid is critical to the future of high index immersion lithography.

Since current resist and topcoat materials have been optimized for water immersion, the switch to organic high index fluids (with considerably different polarities, surface tensions, and viscosities) will have a potentially significant impact on material and lithographic performance. This talk will address what we have learned about a few of these issues, including the effect of fluid on PAG extraction, evaporation and staining, film pulling and scan rate, and topcoat materials design. Finally, lithographic performance obtained with water and organic high index fluids will be compared using a 193 nm interferometric exposure tool.

High-Index DUV Optical Materials

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The limited choice of precision optical materials for the DUV is recognized as a bottleneck for extending 193 nm immersion lithography to its theoretic resolution limits. For plane parallel resist-fluid and fluid-lens interfaces, the numerical aperture of an immersion system is limited by the lowest index of the resist, fluid, and final lens. While the use of water as an immersion fluid is expected to enable practical numerical apertures near 1.3, the promise of further extension using higher-index fluids is thwarted by the lower indices of the lens materials, calcium fluoride and fused silica. Simulations have demonstrated that if lens materials with indices above 1.8 were available, numerical apertures could be extended to greater than 1.55. This could be achieved without substantial increase in the size of the lens system. Numerous of 193 nm-transparent, high-index, isotropic materials exist, but they have not yet been exploited for precision optics. In this talk I survey these materials and their optical properties, focusing on their most troublesome characteristic, the high magnitudes of their "intrinsic" birefringences. The most promising of these oxide materials, the garnets, may be exceptions. Their highly symmetric, yet very complex unit cell structure uniquely constrains their intrinsic birefringences to potentially manageable levels. The wide variety of garnets possible provides a number of potential candidates. At least one candidate garnet, $Lu_3Al_5O_{12}$, is manufactured commercially for dopant hosts for solid-state lasers. The garnets expected to have the smallest intrinsic birefringences, the silicate garnets, in fact constitute important geological components of the earth's mantle and are prized as gemstones. Though nature produces them readily, they are difficult to grow commercially. Germanate garnets comprise a class that may be feasibly manufactured. I discuss the potential for these candidates to be developed into lithography materials. Though high material quality fabrication will be a major challenge, these materials offer a credible route extending 193 nm lithography to 32 nm feature sizes.

Applied Image Computing for Computational Lithography

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While the IC industry is planning to use 193nm wavelength scanners for the foreseeable future, there are two levers that are significantly improving the resolution and manufacturability of ultra sub wavelength IC patterns. One is improving numerical aperture of the wafer scanners by using immersion, the other is improving the patterning process by computational lithography.

Computational lithography is the process of creating and applying full chip scale lithography process models to enable the production of integrated circuits. After an IC chip design layout is complete, but before the final photomask data is output, IC manufacturers use computational lithography to apply and verify appropriate pattern proximity corrections and sub-resolution assist features to full-chip layouts – processes often referred to as model-based SRAF placement, model-based RET/OPC and model-based RET/OPC verification.

Since computational lithography is applied on all critical layers, the exact dimensions and placement of every critical feature is determined by the accuracy of this process. The accuracy of the computational lithography process and is now one of the largest factors in the wafer manufacturing error budget.

To achieve the highest accuracy, computational lithography must model, correct and verify each of the physical lithography processes including mask manufacturing, mask type (PSM) and mask (3D effect) imaging, wafer scanner illumination shape, polarization, and projection optics, scanner exposure and focus variations, photoresist exposure and development, and dry etching.

Recently, image computing has been applied successfully to the tasks of computational lithography. Previously, computational lithography has been performed using the vector or polygon-based representations of the circuit layouts used in IC design. In this traditional approach, there has been a significant trade-off required between computation speed and accuracy. Now, significant speed and accuracy benefits have been achieved by incorporating image-based layout representations and computational algorithms into the computational lithography processes.

Re-mapping appropriate portions of the computational lithography problem into an image-based approach allows the application of repetitive pixel or grid-based calculations to be paralleled and pipelined into dedicated computing boards. The combination of the image-based approach and high speed dedicated computing hardware - familiar to the IC industry in the high speed computing used for image-based wafer and reticle inspections - is "Applied Image Computing."

Several problems have significantly benefited by using applied image computing for computational lithography. The earliest example is full-chip RET/OPC verification. In this task, the adoption of applied image computing improves coverage and eliminates missing lithography failures caused by printing side-lobes. The accuracy and speed of applied image computing has also enabled RET/OPC verification to include wafer scanner focus and exposure variations. RET/OPC corrections that work at nominal process conditions, but fail with anticipated wafer scanner focus and exposure variations can be detected and returned for OPC rework. The most recent application of image computing to computational lithography is in model-based assist bar placement and OPC correction.

Image computing can also be applied for photomask writer proximity effect corrections and other applications both inside and outside the IC industry.

Ultrathin Resists for Immersion and EUV: Reflectivity Control, Integration and Fundamental Issues

Ralph R. Dammel,

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As a corollary to the shrinking of feature sizes along the roadmap, photoresist thickness is also decreasing at a rapid pace. There are two main drivers for this development: the improvement in focus budget possible with thinner resists, and the capillary-pressure driven collapse of resist structures during development. While immersion lithography will bring some relief on the depth-of-focus side, the collapse issue continues to become more severe. Without the use of surfactated rinses, 45 nm structures in 193 nm photoresist collapse at thicknesses larger than 90 nm. From an analysis of resist collapse using an elastic beam bending model, it is predicted that for 32 nm node, collapse will occur at aspect ratios lower than two. While specialized rinse solutions can help abate the collapse issue, we will still have to prepare for very low resist thicknesses in the future.

Thin resists will require different integration schemes, since their dry etch resistance is going to be insufficient for patterning conventional BARCs and even hardmasks. One way forward is to increase resist dry etch resistance, and recent work will be reported on the replacement of the current C_{10} adamantane-based 193 nm resist platform with one based on the next higher section of the diamond lattice, i.e., monomers based on the C_{14}-fused ring system diamantane. On the BARC side, solutions will have to accommodate the antireflection challenge posed by the wide range of angles in high NA lithography as well as provide viable options for dry etch patterning. The paper will report on recent work on Si-containing BARCs and carbon-rich spin-on underlayers which together form a cost-effective, spin-on trilayer system. While the antireflective properties of such as system will not be needed for EUV, it will still solve the integration issues expected for very thin EUV resists. The paper will conclude by comparing different options and evaluating possible paths forward.

Lithography Using the Evanescent Field - Is it Worth the Frustration?

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As optical microlithography continues to be driven into sub-wavelength regimes, the importance of the energy that is evanescent at surface interfaces and near small openings becomes an interesting expansion of conventional imaging limited by diffraction. The true limits for optical lithography become more dependent upon materials and engineering challenges rather than on physics. In this presentation, we will show how lithographic imaging can be enhanced or extended by making use of energy which is normally evanescent. By assembling a projection imaging system based on an ArF excimer laser and sapphire as a final optical element, we have been able to image to 0.13λ (26nm) at 1.85NA in image media with a refractive index lower than needed for propagation. As the numerical aperture of the system is increased beyond the refractive index of the photoresist, the ability to perturb the evanescent field through frustration is removed as would seem the ability to detect or record an image. We propose several mechanisms for this effect, including the perturbation of counter-propagating evanescent fields, the scattering by the small PAG "particles" in the resist, and the ability of the PAG to capture a photon with sufficient dwell time compared to the PAG size. Figure 1 shows an example of what we refer to as evanescent wave lithography (EWL) at numerical apertures of 1.85 and 1.75 for resolution of 26nm and 27.5nm half-pitch, respectively.

We have expanded concepts of evanescent wave propagation for application to a photomask and describe the enhancement using evanescent wave assist features (EWAF). As mask dimensions approach the sub-wavelength scale, the surface-confined evanescent energy needs to be considered together with the propagation of diffracted energy into free space. The portion of the illuminated energy that becomes evanescent increases as mask features shrink. To study this contribution toward photomask enhancement, a series of assist structures were designed for simulation using a FDTD model. Figure 2 shows the layout of an opening in a photomask, flanked by grooves patterned into the mask substrate. When the grooves period is sub-wavelength, a zero-order diffraction grating is formed, forcing all other energy to be evanescent in the glass-thin film interface. Each groove launches an evanescent wave which will decay exponentially but also travel along this interface perpendicular to the main space opening. If added constructively, the total composite field can increase with each successive interaction. When encountering an opening, the amount of energy that is transmitted is modulated based on the phase interference between the composite fields, increasing the intensity and contrast of the opening. We will show how this effect can be employed as a reticle enhancement method to improve the imaging of contact hole features and space openings.

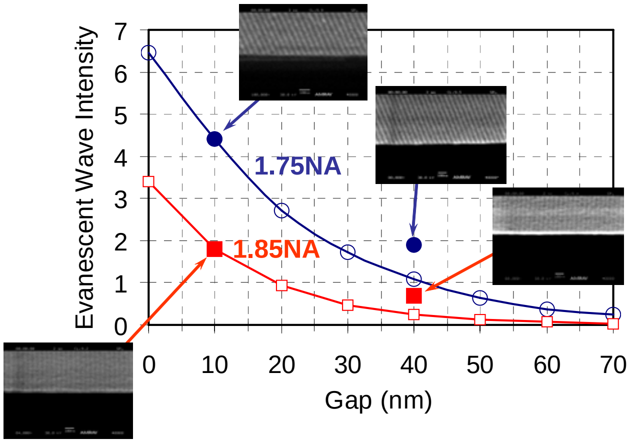

Figure 1. EWL imaging in resist at 1.75NA and 1.85NA.

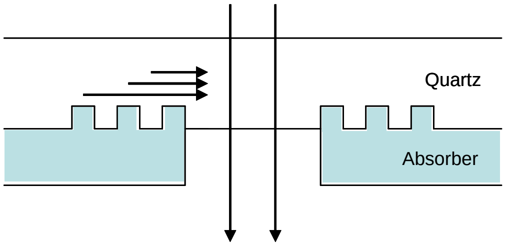

Figure 2. Design of evanescent wave assist features (EWAF) to enhance the near field transmission of a nearby opening.

Wednesday Evening, August 2, 2006
Technical Session 4
Prince Room
Session Chairs: Brian Grenon, Chris Ober

7:15 PM	**ANNOUNCEMENTS**		
7:20 PM	**Roger French**	**Dupont**	**Second Generation Fluids For 193 nm Immersion Lithography: Optics, Imaging and Fluid Lifecycle**
7:45 PM	**Chris Progler**	**Photronics**	**Masks for TFT LCD Lithography**
8:10 PM	**Tsutumu Shimokawa**	**JSR**	**Recent Progress of ArF Lithography Materials Development**
8:35 PM	**Tom Wallow**	**AMD**	**Line Edge Roughness in 193nm Resists: Lithographic Aspects and Etch Transfer**
9:00 PM	**Dan Pickard**	**Stanford University**	**Options for High-speed Electron-beam Lithography**
9:25 PM	**END SESSION**		

Second Generation Fluids for 193 nm Immersion Lithography: Optics, Imaging and Fluid Lifecycle

Roger H. French, Aaron L. Shoe, Robert C. Wheland, Hoang V. Tran, Weiming Qiu,
Jerald Feldman, Steve J. McLain, Min K. Yang, Michael F. Lemon, Doug J. Adelman,
Michael K. Crawford
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Currently water is the first generation immersion fluid for 193 nm immersion lithography. With its refractive index of 1.436 and optical absorbance of 0.036/cm at 193 nm, water immersion technology can enable stepper numerical apertures of 1.3 and optical lithography for the 45 nm half-pitch node of the ITRS roadmap assuming one can utilize a k1 of 0.30 in production. However, in order to achieve higher numerical apertures and thereby go beyond the 45 nm node, 2nd generation immersion fluids are required with 193 nm refractive indices of 1.65.

We have identified three fluids that appear attractive for use as 2nd generation immersion fluids and have previously demonstrated hyper-NA imaging of 32 nm 1:1 lines and spaces using interferometric immersion imaging with an NA of 1.5 and a k1 of 0.25.[1] All three 2nd gen. Fluids simultaneously offer 193 nm refractive indices ranging from 1.64 to 1.66 in combination with 193 nm A/cm values < 0.15.

Our studies of second generation immersion fluid candidates are moving beyond the discovery phase, and into addressing issues for their commercial application. Thus, we continue work to examine and fundamentally understand fluid transparency and refractive index, to fully optimize these properties. At the same time, we are now examining other process concerns, including index variation with temperature, new imaging performance studies, fluid handling considerations, and fluid property maintenance with active recycle during lithographic exposure. The systems and procedures we have developed in these areas continue to show our fluids' promise for sub-45nm immersion lithography applications.

1. R. H. French, et. al., JM3, Topical Issue on Hyper-NA Imaging, July 2005.

Masks for TFT LCD Lithography

Chris Progler and Pat Martin
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In this presentation, we will highlight similarities and differences in mask technology for the IC and TFT LCD applications. Specifically, technology for IC masks tends to be driven by the need for continuously smaller features held to tighter dimensional and placement tolerances while LCD masks are pushed primarily by the need for expanding substrate size and mask usage efficiency. In the context of this comparison, we will touch upon drivers for changing the lithographic reduction ratio in IC and LCD patterning steps.

Focusing further on the LCD photomask, we will review the roadmap drivers for LCD masks and discuss the state of the art in LCD mask fabrication. The important role mask technology plays in reducing the total number of patterning layers required to manufacture a TFT LCD panel will be described as well. Toward this, novel mask making techniques that allow multiple lithography levels to be combined into one masking level will be highlighted.

Finally, we will give a description of cost drivers in the LCD mask application and discuss future trends in mask technology for the fabrication of display devices.

Recent Progress of ArF Lithography Materials Development

Tustomu Shimokawa, Yoshikazu Yamaguchi, Jun-ich Takahashi, Shiro Kusumoto,
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The immersion ArF lithography seems to be the main technology for the device manufacturing below 65nm node. Due to the completely different exposure environment compared with dry exposure system, some of new lithography materials should be necessary to avoid manufacturing issues, such as defects or tool damages. Also, the CD requirement, especially below 45nm node device, does not allow the resist aspect ratio higher than about 2.5 from the view point of the pattern collapse and litho-margin and which will cause the other issue for etching process. All those things are suggesting that some set of new materials development should be needed for the success of devices manufacturing below 45nm node by the immersion lithography technology. We have been focusing each potential issues for years and developing and seeking new materials for the solution. In this paper, we will review the series of ArF lithography materials development in JSR for immersion generation.

Line Edge Roughness in 193nm Resists: Lithographic Aspects and Etch Transfer

Thomas Wallow*, Alden Acheta, Adam Pawloski[†], Scott Bell, Brandon Ward,
Cyrus Tabery, Sarah McGowan, Yuansheng Ma, Bruno LaFontaine, Ryoung-han Kim, and
Harry Levinson

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The performance characteristics of transistor gates degrade as the magnitude of line edge roughness (LER) on the gate increases. The effect becomes increasingly problematic as the critical dimension (CD) of the gate decreases. LER originates in lithographically patterned chemically amplified photoresists and is transferred to underlying substrates during etching. Major efforts to understand and minimize the magnitude of LER in patterned resist features and in patterned substrates are ongoing. We describe a method to determine transfer functions for line edge roughness (LER) from the photoresist pattern through the etch process into the underlying substrate. Both image fading techniques and more conventional focus-exposure matrix methods may be employed to determine the dependence of photoresist LER on the image-log-slope (ILS) or resist-edge-log-slope (RELS) of the aerial image. Post-etch LER measurements in polysilicon are similarly correlated to the ILS used to pattern the resist. From these two relationships, a transfer function could be derived to quantify the magnitude of LER that transfers into the polysilicon under layer from the photoresist. The utility of this method to multiple photoresist and etch processes will be explored.

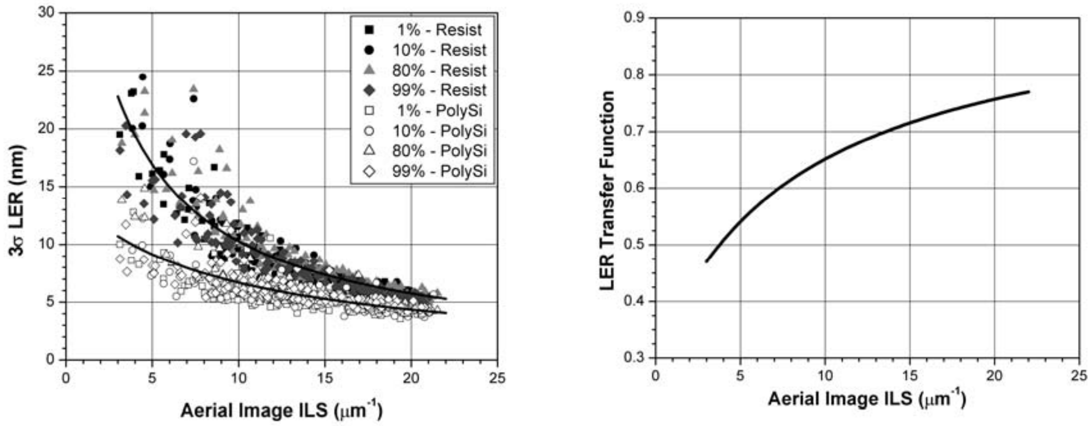


Figure 1. LER of photoresist features and polysilicon features correlated with ILS (left); corresponding LER transfer function (right).

Options for High-speed Electron-beam Lithography

Daniel S. Pickard[1], R. Fabian Pease[1], Timothy R. Groves[2]
1 - Stanford University, 2 - Vistec Corporation

It is well known that space charge (aka coulomb interactions) effects limit the throughput available in a charged particle lithography tool that employs optics that features a single axis. This was well set out by L. Han (PhD dissertation, Stanford University, 2000) who formally quantified the third order aberrations introduced by the space charge. For 32 nm features requiring 10,000 electrons/ minimum feature (Kruit, EIPBN 2006) we need a current of 160microamps to achieve 1 cm2/s throughput. Even for a distributed image (as in electron projection lithography) this can only be achieved with an impractically short focal length final lens. One approach is to introduce correcting elements into the column. An example is the Canon Correction Lanes Array (CLA) configuration. But this avenue does not appear to be being followed. So that leaves only the options of systems featuring multiple axes and there are several approaches to achieving multiple axis electron optics to avoid the space-charge problem.

The original multi-axis approach, Electron Image Projection System (ELIPS), dates from the mid sixties (O'Keefe at al. IEDM 1967) and consists simply of uniform magnetic and electric fields for accelerating and focusing photoelectrons from the clear areas of a photomask onto the resist coated wafer in a manner very similar to a night vision tube. Although working circuits were made with such systems they suffered from outgassing of the resist affecting the photoemitter and from the difficulty of assuring accurate overlay over the whole wafer; especially as the wafers became larger. Multi column approaches were then addressed. The mini-columns pioneered at IBM in the late 80's and developed subsequently at ETEC and most recently at NovelX is the best known approach and recently have shown promising results (L. Muray EIPBN 2006). Other companies such as Multi-Beam Systems (N. W. Parker et al., Scanning 2005) are also active in this area.

In almost a throwback to the original ELIPS idea two projects were spawned in the late 90's . One 'MAPPER' (http://www.mapperlithography.com/) originally employed a photocathode but has since undergone significant changes and is described elsewhere at this meeting. The other 'DIVA' originally employed a variably-shaped electron beam from a photocathode. A less ambitious version, Distributed Fixed Aperture (DIFA), is being developed by us. In this configuration an array of externally modulated laser beams illuminates a photocathode. Each beamlet is accelerated and focused by the uniform magnetic and electric fields onto an array of sub-50nm apertures. Each aperture forms a secondary source of 50KeV electrons that are focused onto the wafer by the uniform magnetic field. Thus the cathode is shielded from the resist-coated wafer. The aberrations of the optics are very low; resolution of <20nm is possible if the secondary sources can be made sufficiently small. We have demonstrated sub50nm resolution. One key problem is stitching the patterns from adjacent beamlets. To facilitate this we have developed a multi-channel secondary electron detector which, together with feedback from the wafer (see, for example, SPLEBL Goodberlet et al., JVST 2002), can be used to assure accurate beam placement. One advantage of the multi-channel secondary electron detector is that it enables DIFA to be used for high speed scanning electron microscopy. Perhaps the biggest remaining difficulty is engineering a suitable primary source of electrons. Various photocathodes have been examined. One featuring resonant surface plasmons is particularly appealing.

Thursday Morning, August 3, 2006
Technical Session 5
Prince Room
Session Chairs: Tim Brunner, John Bruning

8:00 AM	**ANNOUNCEMENTS**		
8:05 AM	**Eli Yablonovich**	**UCLA**	**Plasmonics, Optical Frequencies but with X-ray Wavelengths**
8:30 AM	**Reiner Garreis**	**Carl Zeiss**	**Catadioptric Optics Enabling Ultra-high-NA Lithography**
8:55 AM	**Dario Gil**	**IBM**	**How to Answer Lithography DfM Questions**
9:20 AM	**Hank Smith**	**MIT**	**Zone-Plate-Array Lithography; for Mask Making, Research and Low- Volume Production**
9:45 AM	**BREAK (30 min)**		
10:15 AM	**Bill Arnold**	**ASML**	**Prospects And Challenges for Double Exposure /Double Patterning**
10:40 AM	**Daniel Lopez**	**Bell Labs**	**MEMS-based Spatial Light Modulators for Optical Maskless Lithography**
11:05 AM	**Caroline Ross**	**MIT**	**Block Copolymers as Self-Assembled Masks for Nanolithography**
11:30 AM	**Hiroshi Ito**	**IBM**	**Material Design for Step-and-Flash Nanoimprint Lithography**
11:55 AM	**Patrick Martin**	**Photronics**	**If Mask Makers Ruled the Universe**
12:20 PM	**END SESSION**		

Plasmonics, Optical Frequencies but with X-ray Wavelengths

Eli Yablonovitch, Josh Conway, Shantha Vedantam, & Hyojune Lee
UCLA Electrical Engineering Dept.
Los Angeles, CA 90095-1594

Light waves running along metal surfaces can have some unusual properties. The effective refractive index n can become very large, n>100, leading to optical wavelengths as short as nano-meters. This is the emerging field of plasmonics. It is expected that it will be possible to concentrate optical energy down to a volume of a few nano-meters, while suffering insertion losses of only ~3dB. One of the applications is toward massively-parallel, scanning, maskless lithography.

Plasmonics marks the beginning of optical frequency metallic wiring and circuits. The unusual dispersion relation, and short wavelengths, result from an additional contribution to the inductance, (sometimes called kinetic inductance), owing to the inertia of the electrons carrying the high frequency current. Other than that one modification, the behavior is that of ac electric circuits, with distributed capacitance and inductance.

Among the applications that are envisioned, in addition to nanometer scale scanning maskless lithography, is the nano-meter scale concentration of optical energy for Heat Assisted Magnetic Recording, (HAMR). Magnetic hard disks will soon need a temperature assist for re-writing the nano-domains where the information is stored. Another application that is expected to emerge is nano-scale components that are extremely non-linear but that require very little energy to operate. In effect, this would be a type of “optical transistor”, but based upon metallic wiring.

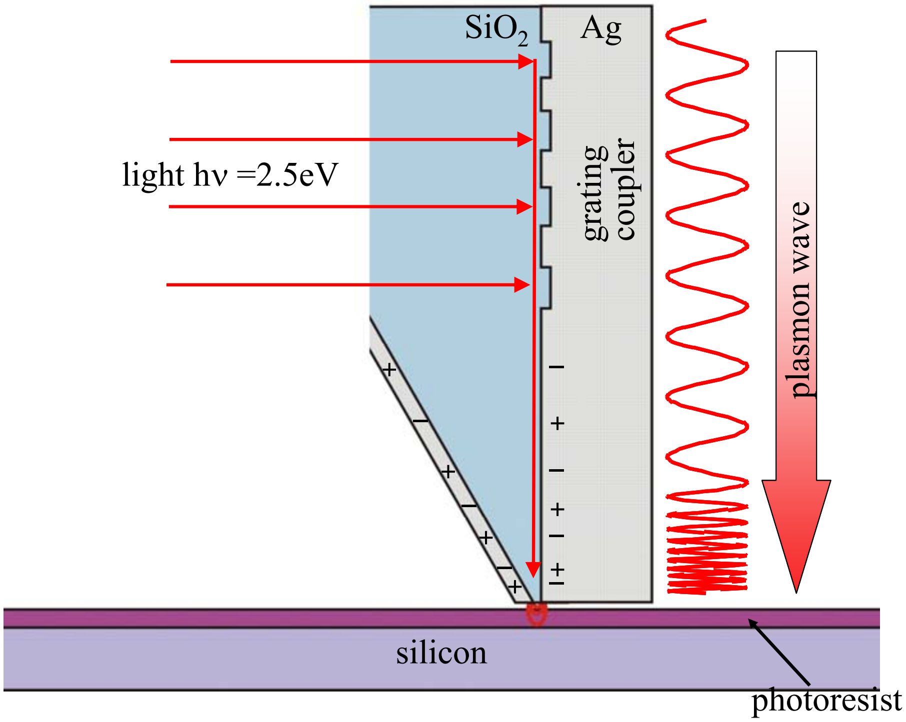


Figure 1: Focusing structure for scanning maskless photolithography. The optical wavelength gets shorter and shorter in the tapered plasmonic waveguide.

Catadioptric Optics Enabling Ultra High NA Lithography

Reiner Garreis,
Carl Zeiss SMT AG
73446 Oberkochen, Germany

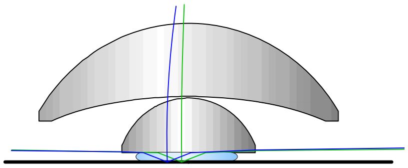
To enable optical lithography for sub 50 nm features, ArF immersion lithography requires numerical apertures to be significantly larger than 1 - thus leading to new challenges for optical design.

Here we demonstrate that traditional approaches based on refractive lens designs are not adequate to capture these extreme etendues due to exploding size of the lens elements (and thus cost) and increased optical sensitivities.

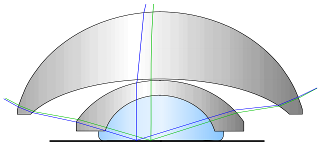
Catadioptric lens designs can overcome these fundamental issues. Various catadioptric design approaches will be discussed and a detailed assessment will be presented. The main criteria used to evaluate the potential of the presented solutions include inline and folded design types, reticle compatibility, impact of mirror designs and mirror coatings, optical sensitivities, polarization capabilities and image field shape.

Using the design type called Catadioptric Inline Design, which realizes the NA of 1.2, we will demonstrate the superior performance capabilities of such systems in terms of wavefront, straylight and polarization and by that the low k1 imaging down to 45 nm half pitch and the extendibility to NA 1.3.

Immersion with high index fluids



Max NA ~0.9 x min (n_{glass}, n_{fluid})
Requires new high index glass
& high index immersion fluid



Max NA ~0.9 x min (n_{fluid})
Requires very low absorption
high index immersion fluid

The fun part of the talk will be estimates and speculations on how high ultra high NA might become using these design types together with new immersion fluids and new optical material as well as how far the lithography roadmap can be driven by those estimates.

How to Answer Lithography DfM Questions

Dario Gil, Scott Mansfield
IBM Semiconductor Research & Development Center
Hopewell Junction, NY 12533

Ever since the development of the first accurate semiconductor process models, the dream of creating a "Virtual Fab" is something that has been proposed and pursued by a wide variety of players within the semiconductor industry (i.e. the EDA industry, the fabless customers, the foundries, the IDMs, universities, etc). The idea is plausible enough: The intersection of increasingly accurate modeling of the actual process by which semiconductor devices are fabricated (e.g. lithography, etch, etc), and access to fast computers, can enable the creation of a "virtual fabrication process" that can be used to optimize designs, shorten cycles of learning and achieve a faster time-to-market. While implementing this vision is a decades-long effort, the advanced simulation technologies that have been developed in years past have already altered the way semiconductors are designed and built (Model-Based Optical Proximity Correction –MBOPC- and Optical Rules Checking –ORC- are two particularly successful examples).

This talk will present an assessment of the status of the "virtual fab" concept and will discuss one of the key remaining challenges for full implementation, namely, the integration of the wide variety of point simulation tools and compute platforms into a unified predictive model. Examples will be presented in which ever more complex DfM questions are being answered by incorporating multiple simulation models and hardware platforms, ranging from simple stand-alone computers to the world's most powerful supercomputer (BlueGene). A brief discussion of the economic implications of the "virtual fab" will also be addressed.

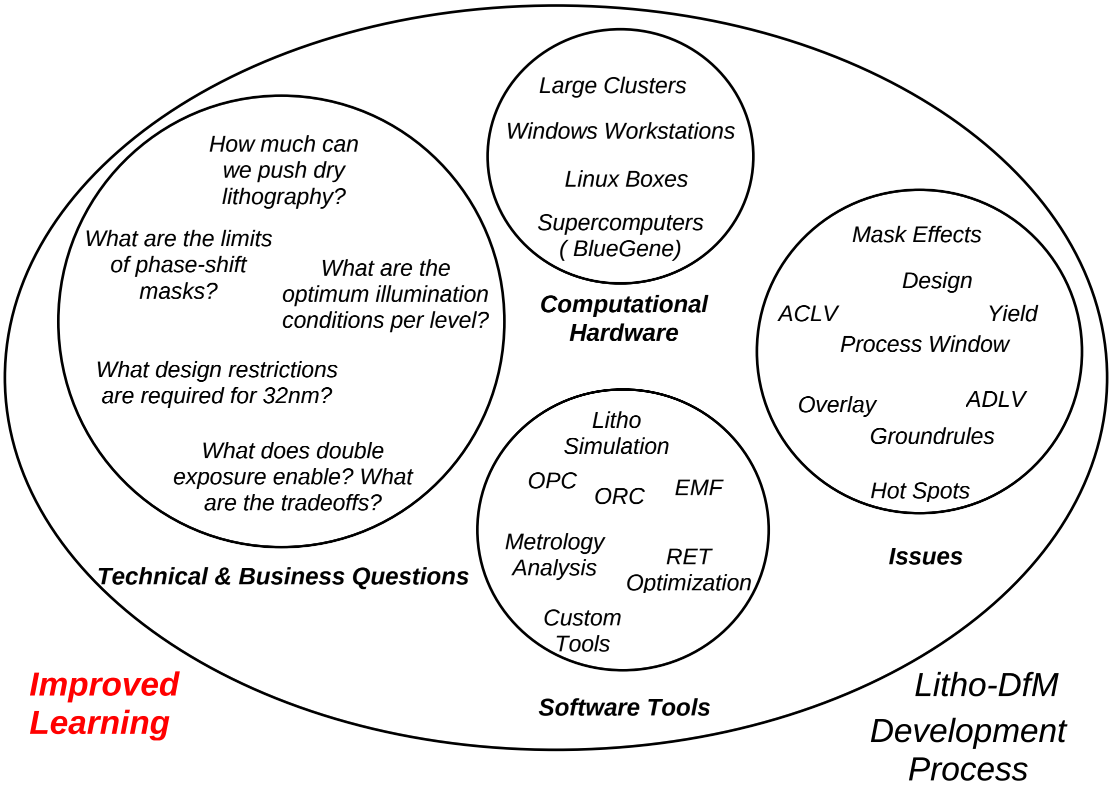


Figure 1. Illustration of the complexity of the lithography-DfM development process. A proper analysis of the technical & business questions that emerge as part of the semiconductor manufacturing process requires the proper consideration of a wide variety of key process issues that need to be analyzed with the right software tools and computational hardware.

Zone-Plate-Array Lithography; for Mask Making, Research, and Low-Volume Manufacturing

Henry I. Smith[1,2], Rajesh Menon[1,2], Michael Walsh[2] and Feng Zhang[2]
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and
[2]Lumarray, Inc.
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Somerville, MA 02143

The availability of low-cost computing, high-speed electronics, spatial-light modulators, precision stages and techniques for accurately fabricating diffractive optics (e.g., Fresnel zone plates) have combined to enable an entirely new approach to maskless lithography based on dot-matrix printing, illustrated in Fig. 1. This scheme, zone-plate-array lithography (ZPAL), circumvents the limitations imposed by approaches based on field imaging (i.e., limited field sizes, distortion, aberrations, and constraints on materials, wavelength, and coherence) and achieves dense patterns of arbitrary geometries down to k1 = 0.29. To make this tool available to others for research, mask making and low-volume manufacturing we have spun-off from MIT a company, Lumarray, Inc., which will have a working prototype, the ZP-150, available in August 2006. High speed writing is achieved through the use of 1000 (or more) diffractive lenses operating in parallel. To achieve sub-30 nm feature sizes one can either go to shorter wavelengths or pursue an entirely new approach based on material nonlinearities called Absorbance-Modulation Optical Lithography (AMOL). The short-wavelength approach (i.e., deep UV, EUV or x-ray) is favored by the use of diffractive optics, however it is constrained by the availability, cost and reliability of CW sources in those wavelength ranges. The AMOL approach, on the other hand, performs a compression of the point-spread-function via photochemistry, and promises resolution better than 1/10th the wavelength. Current research at MIT, aimed at perfecting AMOL, will likely prove once again the advantages of photons over charged particles for lithography.

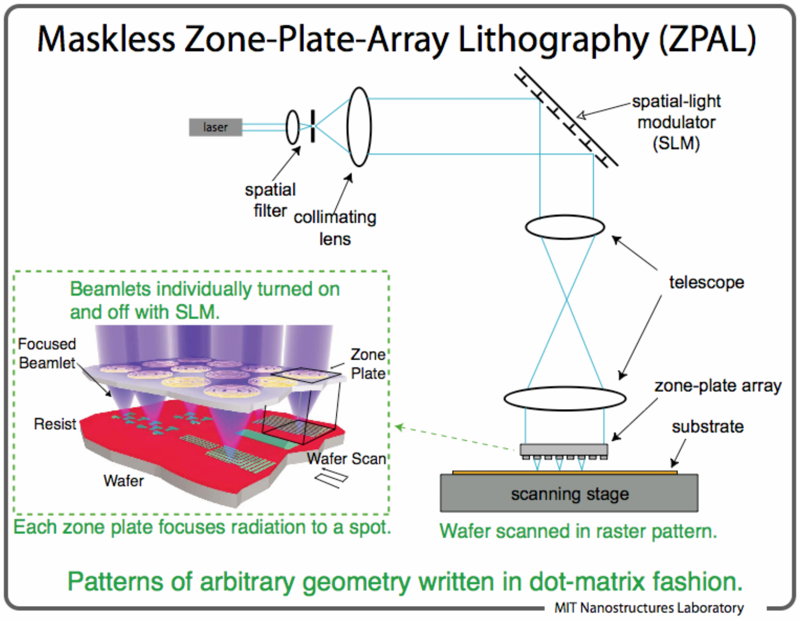


Fig. 1: Schematic of zone-plate-array lithography

Prospects and Challenges for Double Exposure-Double Patterning Lithography

William H Arnold, Mircea Dusa
ASML Technology Development Center

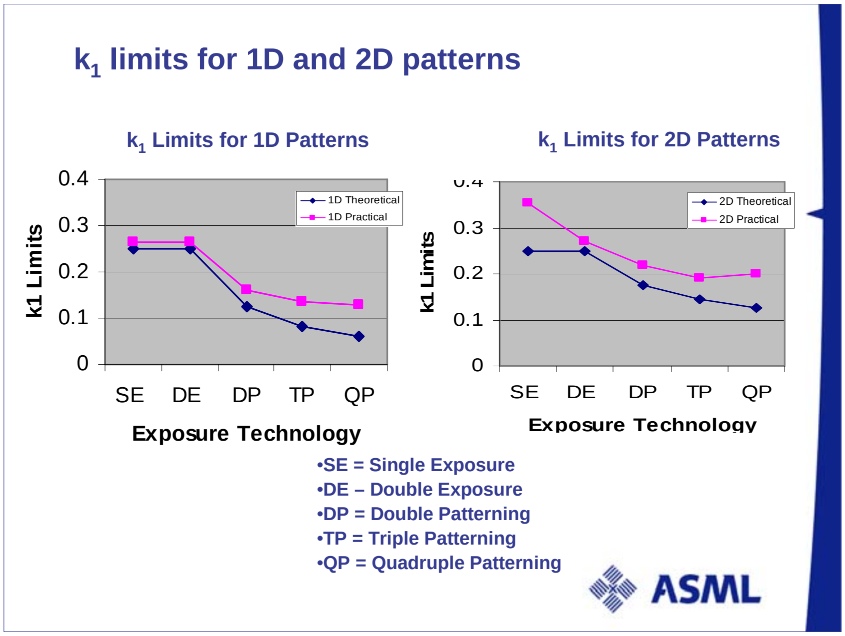
Rapid expansion in mobile memory devices requires lithographic patterning capability that is beyond the resolution limit of ArF water-based immersion tools. In recent years, attention has been drawn to the possibility of using double exposures and double patterning processes to extend the life of ArF lithography.

The limit of resolution in a single exposure for dense lines and spaces is well known to be $k_1 = 0.25$ where $k_1 = NA\ \lambda / R$, and R is the half pitch. For 2D patterns such as dense contact holes, the theoretical limit is again 0.25, however, in a practical sense when dose, focus, and mask errors are taken into account, the practical limit is near k_1 0.354, using quasar type illumination.

Double exposures (two litho steps, followed by one etch) have been used for years to define small gates with excellent CDU using a phase edge and trim mask. Double exposure does not allow one to beat the k_1 0.25 resolution limit for dense features, however it does allow for more process latitude in defining difficult 2D structures and controlling end of line behavior.

Double patterning (litho/etch followed by litho/etch) does allow the effective k_1 limit to be broken, and it is possible to approach k_1 0.125 for lines and spaces, and 0.177 for dense contacts. Practical limits are set by error budgets for dose, focus, and mask CDs, as well as overlay error between the first and second exposures. Adding further litho/etch steps can theoretically provide further subdivision of features, but the practical error budgets limit this in practice. See Figure 1 for the theoretical and estimated practical limits of k_1 for 1D and 2D features.

This presentation will give an overview of applications for double exposure and double patterning processes, and will show experimental results demonstrating < 40nm double patterning capability on a dry 0.93NA ArF scanner.



k_1 limits for 1D and 2D patterns

- •SE = Single Exposure
- •DE – Double Exposure
- •DP = Double Patterning
- •TP = Triple Patterning
- •QP = Quadruple Patterning

Figure 1 – k_1 limits for one dimensional and two dimensional mask patterns

MEMS Based Spatial Light Modulator for Optical Maskless Lithography

D. López, V.A. Aksyuk, G.P. Watson, N. Basavanhally, M.E. Simon, R. Cirelli, F. Pardo, F. Klemens, A. Papazian, C. Bolle, J.E. Bower, E. Ferry, W. Mansfield, J. Miner, T. Sorsch and D. Tennant

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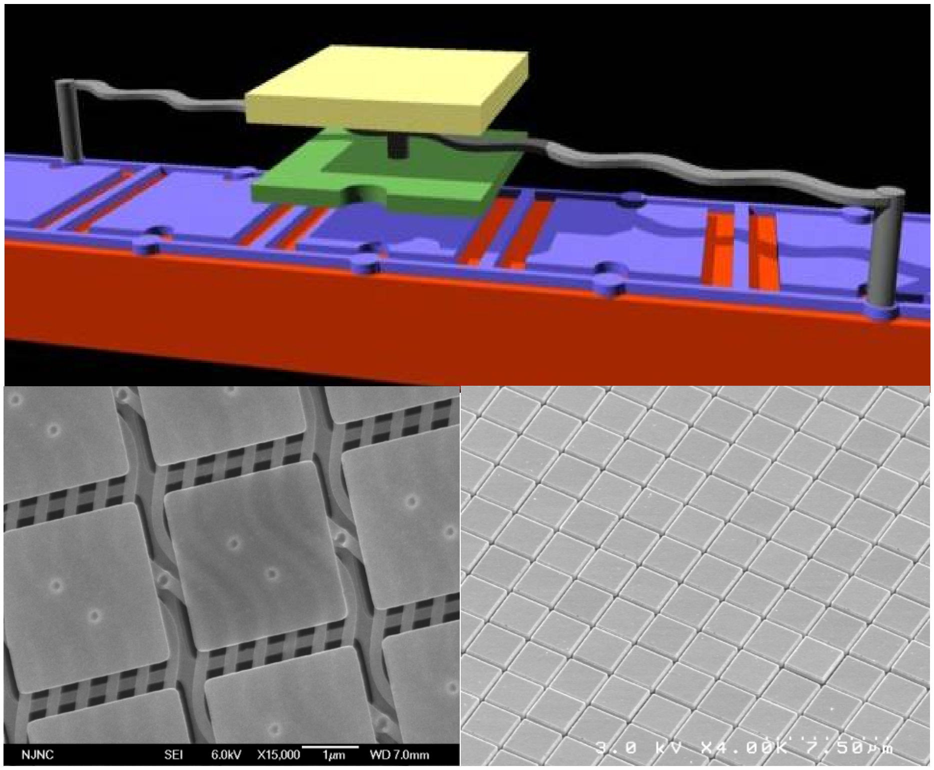
We have fabricated arrays of 512x128 actuated micromirrors to modulate Deep Ultraviolet (DUV) radiation for Optical Maskless Lithography (OML). The arrays consist of micromirrors having 3um and 5um lateral dimension and 90% optical fill factor. The vertical position of the mirrors is continuously controlled by electrostatic forces allowing us to vertically displace them 80nm with very low tilt and less than 4V. The micromirror typical response time is less than 10 µseconds.

These arrays were fabricated using 193nm optical lithography in a surface micromachining process having 5 structural layers with minimum features as small as 130nm and better than 50nm alignment error.

We have pre-wired our micromirrors and tested them by generating specific patterns (lines, gratings, checkerboards) containing up to 8000 mirrors moving in parallel.

To build a fully functional 10M-pixel SLM we intend to hybridly integrate electronic drive circuits with our mirrors. Low voltage operation that is being described is absolutely critical, since we have to use high density, low voltage CMOS drivers to fit within the extremely small footprint of our pixels.

The micro-mirror arrays we have fabricated are about an order of magnitude denser than the state of the art for a MEMS process of comparable complexity.



Block Copolymers as Self-Assembled Masks for Nanolithography

C.A. Ross, J.Y. Cheng, V. Chuang, F. Ilievski, Y. Jung
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Massachusetts Institute of Technology
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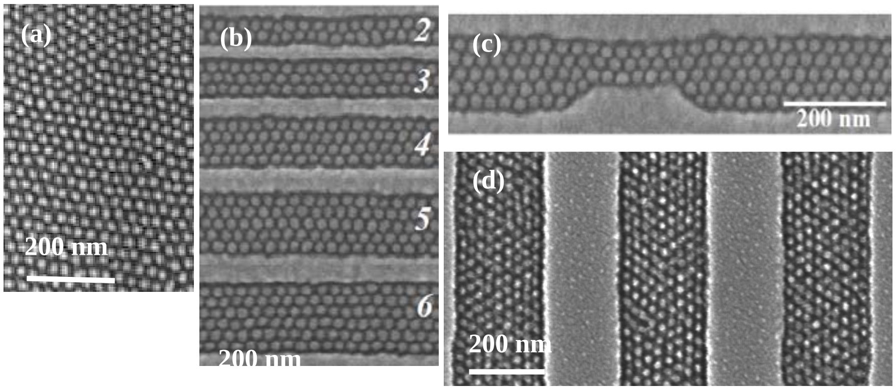
Block copolymers can form self-assembled structures with controllable geometry and periodicity of ~20 nm and above. These structures have therefore been proposed for use as self-assembled masks for nanolithography. In this application, a thin film of block copolymer is spin-coated onto a substrate, and annealed to induce microphase separation. One of the two blocks is then removed to leave a pattern of lamellae, cylinders, spheres or holes, which can then be transferred into a functional layer to form part of a device. The self-assembled polymer pattern typically has good short-range order, but no long-range order, limiting its usefulness in many applications. In this work we will describe the templating of block copolymers using shallow substrate features, which impose long-range order on the block copolymer pattern. Examples of ordered spherical microdomains of polyferrocenyldimethylsilane (PFS) are shown in the figure, after removal of the polystyrene (PS) block from an ordered PS-PFS block copolymer. The polymer period adjusts to be commensurate with the template, allowing a good quality ordered pattern to be formed over a wide range of template widths. For very narrow templates, about equal to the periodicity of the polymer, a single row of spheres can form, with an aspect ratio determined by the template width. We will discuss the capabilities and limitations of this technique, and show examples of magnetic nanostructures patterned using block copolymers.

J. Cheng, W. Jung, C.A. Ross, "Magnetic nanostructures from block copolymer lithography: hysteresis, thermal stability and magnetoresistance", Phys. Rev. B 70 064417 p1-9 (2004); J. Cheng, C.A. Ross, A. Mayes, "Nanostructure Engineering by Templated Self-Assembly", Nature Materials 3 823-8 (2004); J.Y. Cheng, F. Zhang, H.I. Smith, G.J. Vancso, C.A. Ross, "Pattern registration between spherical block copolymer domains and topographical templates", Advanced Materials 18 587-601 (2006). This work is supported by NSF and SRC.



(a) Self assembled block copolymer on a smooth substrate, showing lack of long range order. (b) In shallow grooves, the polymer forms long range ordered structures. (c) More complex structures such as the 5-3-5 pattern can be made in modulated grooves. (d) Ordered pattern transferred into silica to make 100 nm high posts with 25 nm period.

Material Design for Step-and-Flash Nanoimprint Lithography

Hiroshi Ito, Frances A. Houle, Rick A. DiPietro, Mark W. Hart
IBM Almaden Research Center
650 Harry Road
San Jose, CA 95120

As the resolution limit of chemical amplification resists may be approaching and the cost of exposure systems is becoming forbiddingly high, step-and-flash nanoimprint lithography (SFNIL) has been developed as an alternative next generation lithographic technology by Willson (University of Texas at Austin) and Molecular Imprints. Multifunctional acrylates containing Si along with a radical photoinitiator were selected initially as an etch barrier material by UT Austin/Molecular Imprints. However, since photochemical curing through a radical mechanism is rather slow and retarded by oxygen (air), the Willson group investigated cationic curing of Si-containing vinyl ethers, which is faster and insensitive to oxygen. We have initiated a new project to explore the potential of SFNIL lithography and to develop a robust imprint process. We are interested in the use of vinyl ethers as an etch barrier material and have incorporated a number of new inventions in the materials and processes.

Silicon-containing vinyl ethers were prepared and aliphatic divinyl ethers were purchased from Aldrich. The volatility of the vinyl ethers was studied by thermogravimetric analysis. A number of photochemical acid generators (PAG) were screened for their solubility in the vinyl ethers. Selection of PAG was the most important first step of our imprint project as a majority of PAGs developed for use in chemical amplification resists has limited solubility in nonpolar vinyl ethers. Tolyldiphenylsulfonium triflate has been found among ionic PAGs to be soluble in organic vinyl ethers but its solubility in Si-containing vinyl ethers is still limited. We have found that nonionic PAGs developed for use in 193 nm resists by Ciba Specialty Chemical are uniquely suited for use in our vinyl ether formulations. Spectral response of PAGs was investigated and a sensitizer such as 9-anthracenemethanol or phenothiazine was added when the PAG does not absorb at 365 nm (i line). Consumption of the C=C double bond as a function of the exposure dose was studied by FT-IR and by using a differential scanning calorimeter equipped with a UV lamp. The latter technique provided a wealth of information about the cure kinetics including the temperature excursion during photochemical crosslinking. Another important issue in formulating the curing materials was their storage stability. Reflecting the high reactivity of vinyl ether, the formulation solidified within 2 months, within 20 days in some cases, at room temperature. We have identified a couple of compounds, 9-anthracenemethanol and phenothiazine, that can extend the shelf life stability of the vinyl ether curing formulations to >1 year. Thus, these compounds can function as a sensitizer and stabilizer.

The transfer layer employed in SFNIL is typically antireflection coating (ARC), crosslinked by high temperature bake to prevent interfacial mixing with a layer coated on top of it. Thus, it is difficult to strip the transfer layer with solvent after etching of the substrate. The transfer layer material we selected can be overcoated without interfacial mixing and can be stripped readily with a solvent because it is not crosslinked prior to overcoating. We are interested in covalently linking the transfer layer with the etch barrier layer by applying an adhesion promoter. We are also studying the effect of addition of low surface energy compounds in the curing formulation on ease of release of the template after curing.

The film stack after curing was examined by secondary ion mass spectroscopy (SIMS) and by X-ray photoelectron (XPS) spectroscopy. Migration of F-containing compounds to the surface was observed. Etching rates of the cured vinyl ether layer and the transfer layer were measured in fluorocarbon and oxygen plasmas. Imprint experiments were carried out on a Molecular Imprint tool, successfully producing 50 nm 1:1 line/space patterns with an aspect ratio of about two. We are also working on reverse-tone SFNIL.

If Photomask Manufacturers Ruled the Universe…..

Patrick Martin
Photronics (USA)

The ability to predetermine how a photomask may look given the premise that the photomask supplier has the ability to drive the industry forward would have a profound impact not only on the lithography industry but on the semiconductor industry as a whole. In the current state of affairs, the merchant photomask supplier has little ability to change from the conventional wisdom of keeping the tradition alive using archaic principles scaled for todays applications.

This paper will examine the opportunity to address aspects of enabling photomask technology from data treatment through material integration challenges, to equipment infrastructure and final mask integration. In addition, given the opportunity to drive the photomask industry forward, opportunities exist for optimizing the photomask such that the overall cost model breakdown in the supply chain could radically improve. The question is whether or not we are ready for a change and if so, what should be the appropriate focal point items for real consideration.

Details will be provided on photomask process integration aspects and fundamental photomask equipment integration. In addition, is the time right for a mask consortium for collaboration on pre-competitive technology requirements or what are the available alternatives to address relatively near term technology challenges?

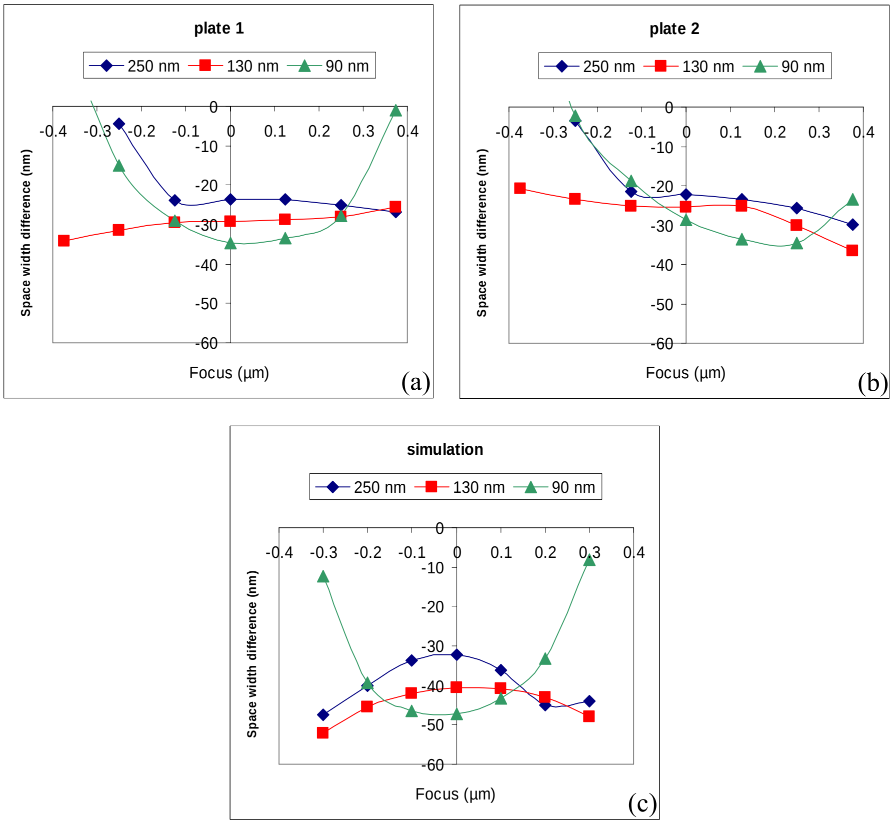


Figure 1 (a)-(b) AIMS result of the space width difference (between 0 and π-shifted space) through focus for 3 different line widths in a dense configuration obtained from two masks with different fabrication processes (early data October 2004). **(c)** Rigorous EMF simulation of the space width difference through focus for 3 different line widths in a dense configuration for an ideal AAPSM without undercut show the global trend seen in (a-b).

Friday Morning, August 4, 2006
Technical Session 6
Prince Room
Session Chairs: Frank Schellenberg, Fabian Pease

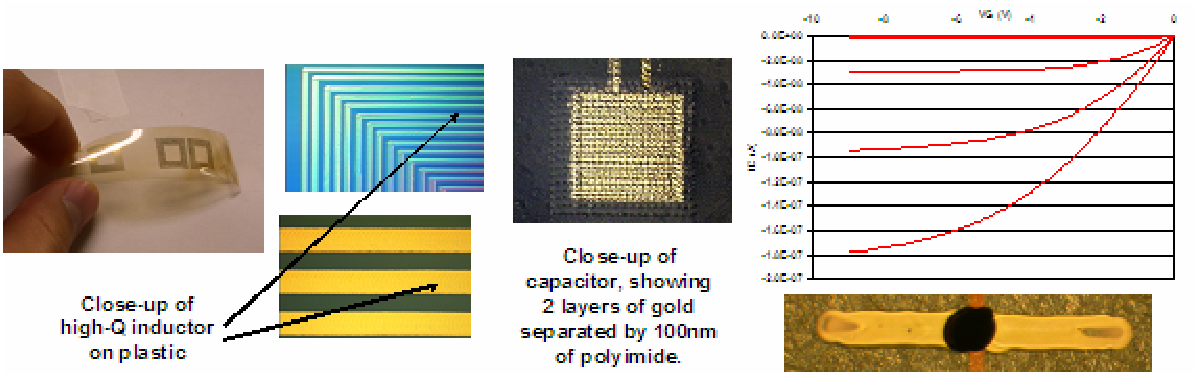
8:00 AM	**ANNOUNCEMENTS**		
8:05 AM	**Vivek Subramanian**	**UC Berkeley**	**Droplet-on-demand Lithography: An Enabling Technology for Low-cost Electronics**
8:30 AM	**Mike Lercel**	**Sematech**	**A Deep Dive into Extension of Immersion Lithography**
8:55 AM	**Takaharu Miura**	**Nikon**	**Nikon EUVL Development Status**
9:20 AM	**Peter Rabkin**	**Xylinx**	**Fabless/Foundry DFM - Challenges and Solutions**
9:45 AM	**BREAK (30 min)**		
10:15 AM	**Hitoshi Sunaoshi**	**Nuflare**	**Enabling Technologies to Extend E-beam Mask Writing**
10:40 AM	**Chuck Black**	**IBM**	**Polymer Self Assembly for Lithography Subdivision in Semiconductor Microelectronics**
11:05 AM	**Bruno LaFontaine**	**AMD**	**Will EUV lithography be limited by the performance of resists?**
11:30 AM	**George Barclay**	**Rohm&Hass**	**A New Materials Approach for 193 nm Immersion Lithography: Defect and Leaching Control**
11:55 AM	**Joe Gordon**	**Toppan**	**Lifting Lithography's Wedding Veil of Haze**
12:20 PM	**END SESSION**		

Droplet-on-demand lithography: An enabling Technology for Low-Cost Electronics

Vivek Subramanian, Alejandro de la Fuente Vornbrock, Steven Molesa, David Redinger,
and Steven K. Volkman
Department of Electrical Engineering and Computer Sciences
University of California, Berkeley
Berkeley, CA 94720-1770

In recent years, there has been substantial interest in ultra-low-cost electronic systems for "disposable" applications such as RFID tags, low-resolution advertising displays, and throw-away sensors. Most of these applications require fixed form factors and have relatively low performance requirements. As a result, printing technology has received a great deal of attention. While printing technology in general has much lower resolution than conventional microlithography technology, it does have several cost advantages. First, many printing platforms offer reduced capital expenditure and increased throughput. Second, printing allows the direct writing of electronic materials, eliminating the need for subtractive processing steps. Third, printing offers excellent compatibility with low-cost flexible substrtates such as plastic. The net result is a tremendous cost advantage for printing, albeit accompanied by much worse linewidth and associated circuit performance degradation. Of the various printing techniques that have been examined for low-cost electronics, droplet-on-demand techniques (i.e., inkjet printing) have received the most attention. Since droplet-on-demand inkjet is a digital input technique, on-the-fly correction for substrate distortion is possible, which is a tremendous advantage when using low-cost substrates. Additionally, inkjet printing typically requires very low viscosity "inks", which allows for the avoidance of binder materials in the inks. This in turn maximizes achievable performance.

In this work, we describe our progress in the development of droplet-on-demand lithography as a viable technique for fabrication of ultra-low-cost electronic circuits. We describe the state of the art of droplet-on-demand lithography, including printing platforms, integration technology, and ink materials technology. Using a combination of nanoparticles and organic materials, we have realized a range of conductor, semiconductor, and dielectric inks and have used these to realize transistors, inductors, capacitors, multilevel interconnects, diodes, etc. Based on the achieved results to date, we discuss the remaining challenges for droplet-on-demand lithography-based low-cost electronics, and identify opportunities for the same in the future.



(left) passive components printing using droplet-on-demand lithography and a range of nanoparticle and polymer inks (right) printed organic transistor fabricated using a similar materials technology

A Deep Dive into the Extension of Immersion Lithography

Michael Lercel[1], Andrew Grenville[2]
SEMATECH, 1 assignee from IBM, 2 assignee from Intel
2706 Montopolis Dr
Austin TX 78741 USA

Understanding the extendibility of 193-nm immersion lithography is necessary for strategic investment decisions about its supporting infrastructure and for the development of competing technologies. The supplier community is now positioned to deliver water-based immersion lithography up to a numerical aperture (NA) of 1.3, appropriate for 45-nm half-pitch patterning. Extending immersion to the 32-nm half-pitch could be enabled by the invention of suitable high-index materials or by the implementation of double-exposure techniques. This paper surveys the requirements of and prospects for high-index immersion fluids, high-index lens materials and high-index resist to meet both an intermediate numerical aperture (NA~1.45) and a full 32nm half-pitch solution (NA>>1.5). We also briefly review double exposure, which poses substantial engineering challenges to chip layout and exposure tool design as well as the process and mask infrastructure. Lastly, the cost of implementing and using these technologies must also be considered. This paper will look at some of the cost drivers and showstoppers of extending immersion lithography.

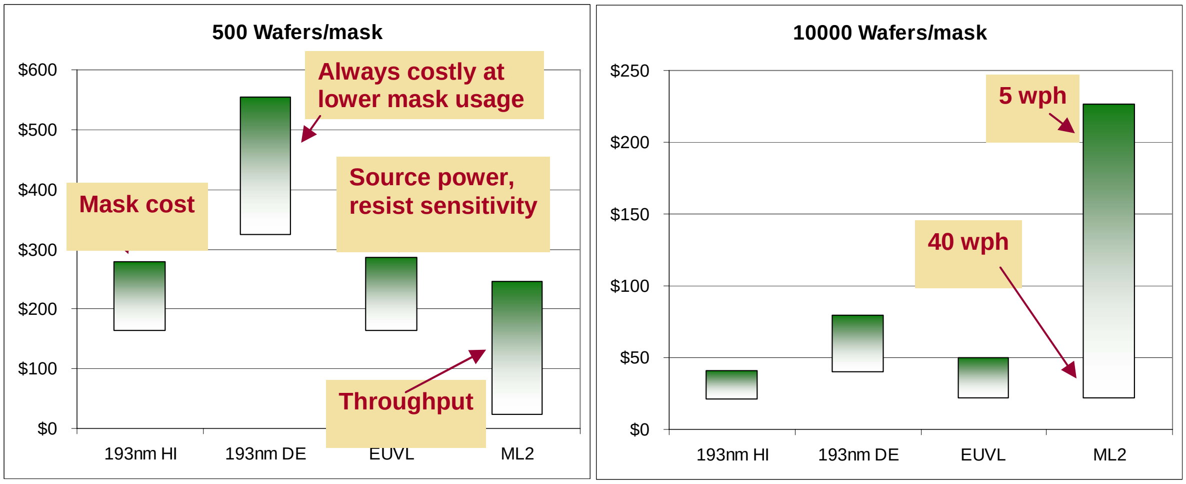


Figure 1. Cost per wafer pass analysis of various lithography options under two scenarios. (Left) 500 wafers/mask usage similar to ASICs and system-on-a-chip mask usage, and (right) 10000 wafers/mask representing medium to high volume manufacturing. The vertical bars represent a range of inputs for mask cost, throughput, and tool cost for each technology.

Nikon EUVL Development Status

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ABSTRACT

Extreme Ultra Violet Lithography (EUVL) is considered as the most promising technology below hp45nm node, following ArF immersion lithography considering trend of achievable process K1 factors. In this presentation Nikon would like to present significant progress on the development of EUV exposure tool showing recent encouraging data of mirror polishing accuracy and particle protection experiment on Nikon reticle protection concept. There are several key important areas which should be developed to realize EUVL to be feasible such as reflective mask, resist, and tool itself. The reflective mask features such characteristics as pellicleless, ultra-smooth blank flatness and defect free. The resist should be of high sensitivity and small line edge roughness (LER) as well as fine resolution. EUV exposure tool itself consists of major important modules such as EUV light source, projection optics, vacuum body, vacuum stages and so on. As far as EUVL optics development is concerned, through the development of high-NA small-field EUV exposure system (HiNA) in conjunction with EUVA (Extreme Ultraviolet Lithography System Development Association) projects, we have developed new polishing technologies such as ion-beam figuring and elastic emission machining, and new high-precision interferometers for aspheric surface metrology. The latest data of high-precision interferometer shows that repeatability of 32nm RMS was confirmed in the measurement of aspherical surfaces. By using a new polishing method, we successfully reduced low-spatial-frequency roughness (LSFR), mid-spatial-frequency roughness (MSFR) and high-spatial-frequency roughness (HSFR) simultaneously. Wave front sensor system has been also developed partly in EUVA project. A new wave front sensor system which can be used for evaluating the projection optics with EUV light has already been installed in New SUBARU synchrotron facility in University of Hyogo. Our multi-layer coating technology has been also remarkably improved. High reflective Mo/Si multi layer coating with low stress has been successfully achieved and irradiation tests using synchrotron radiation have been conducted. Successful achievement of those developments enables us to fabricate high-precision aspheric mirrors meeting the specification for EUV pre-production and process development tool called EUV1.

EUV1 tool system design and its detailed design of all modules such as full-field projection optics module, illumination optics module, vacuum body module, vacuum compatible reticle/wafer stage modules, reticle/wafer loader modules have been completed. Development and prototyping of major modules such as projection optics barrel, vacuum stage modules and vacuum body module have been carried out and the results were reflected in the actual tool design. Nikon has also learned a lot about key factors necessary for reliable vacuum lithography tool system through EPL (Electron Projection Lithography) development program. Improvement areas were identified and reflected into actual EUV1 tool design. Nikon announced to employ Xe DPP EUV light source for EUV1 tool since it is now the most matured technique among various schemes of light sources and the cleaner source than other ones using solid target. Basic source requirements such as power at IF, repetition rate, and Etendue have been specified. Nikon has been also heavily involved in the infrastructure development such as reticle standardization and reticle handling development. Nikon has studied reticle protection method and proposed Dual Pod Concept in cooperation with Canon. Nikon also has been developing its own reticle cover as a method of reticle protection with the support of Nuflare Technology, which is scheduled to be implemented in EUV1 tool.

Nikon has already completed EUV1 module parts fabrication and got into sub-assembly phase of all modules to meet tool development schedule. Proto-typing of projection optics has been proceeded on schedule with NA 0.25, magnification 1/4, and 26x33mm field. Complete set of production and metrology tools necessary for real projection optics production has been completed. EUV1 tool development program has been proceeding along with mask, resist, and other infrastructure developments. Nikon has been taking a strategic development approach to accelerate EUV1 tool development working with more than ten companies and organizations considering the most effective and best risk sharing way.

Nikon announces that EUV1 tool is scheduled to be delivered in 1st half of 2007. Development of production tool dubbed EUV2 is also considered.

Keywords: EUVL, Extreme Ultra Violet Lithography , EUV exposure tool, EUV pre-production tool, EUVA project

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Fabless/Foundry DFM: Challenges and Solutions

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Leading fabless companies currently produce designs for cutting edge technologies almost on par with leading IDMs. Foundries have evolved from producing devices one to three nodes behind IDMs to funding leading-edge R&D and manufacturing those chips using advanced processes. The key foundry/fabless challenge – how to produce manufacturabe designs for cutting edge technology nodes to meet time-to-yield and time-to-volume requirements – is being overcome by an extensive effort to realize fabless/foundry integrated Design For Manufacturability (DFM) [1]. Fabless/foundry DFM requires addressing a number of issues, such as obtaining and utilizing proprietary manufacturing information in the course of design and fabless-to-fab optimization loops. That, in turn, requires addressing the problem of compatibility of EDA tools, data structures, process models, encryption, etc. Solving these issues is paramount for enabling sufficient information flow between design and manufacturing and is critical for the overall competitiveness of the foundry/fabless business model. Therefore, leading design houses, foundries and EDA vendors are aggressively moving into the DFM arena to provide either proprietary or more general answers to the DFM challenges. This is exemplified by recent announcements on the new DFM support "Ecosystem" and DFM "unified" data format by the biggest pure-play foundry TSMC [2].

Since sub-wavelength (λ=193nm) immersion lithography is expected to remain the dominant patterning technology down to at least 32nm, lithography compliance check (LCC) continues to be the key DFM component. The requirements for fabless litho-DFM are (1) integration into design flow DFM procedures that can accurately cover fab's RET/OPC/MDP flow with accurate models, rules and OPC recipe, (2) LCC analysis of all critical layers across process variability window, (3) comprehensive statistics, severity scale and layout mapping of errors. In addition, litho-DFM flow should include optimization loops where the DFM results are obtained and shared between design house, foundry and mask house. Intelligent analysis capabilities are needed to formulate corrective actions: design, process and/or OPC fix. The results drive improvements of physical design, refinement of design rules and DFM requirements, and fine-tuning of design tolerances. They are fed forward to the fab for possible RET/OPC improvements and in-line metrology instructions to monitor, control and optimize litho and etch processes. Simultaneously, design tolerances and hot spot analysis results are fed forward to the mask house for mask requirements optimization. Additional optimization loops involve silicon test structures and product prototypes to calibrate process models and OPC recipe against experimental results to complete verification and optimization of design, process and mask.

A step further is to integrate litho- and non-litho DFM [1]. Non-litho DFM steps need to be performed in conjunction with and in addition to LCC. Litho and CMP impact on pattern fidelity, film thickness, CD uniformity, transistor and interconnect variability examinations are combined with critical path performance, power, and noise analyses to determine optimal performance/manufacturability trade-offs. Potential impact of random defects is assessed by critical area analysis. The intelligent analysis capabilities here are expanded to include all litho and non-litho DFM considerations to formulate conclusions, recommendations and the most optimal course of actions for process, OPC/mask and/or design fix. Capabilities to act upon DFM analysis results are critical, and design automated repair should be an important part of DFM flow. The automated layout repair should preserve layout hierarchy to allow for further design modifications & connectivity checks.

In summary, fabless DFM requires tools, methodologies and flows that would enable information sharing and optimization through the whole chain of design house, mask shop & foundry - still a challenge for all involved.

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Enabling Technologies to Extend E-beam Mask Writing

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Shrinking minimum feature size coupled with aggressive OPC for photomask manufacturing has been and will continue to be the driving force to demand tighter and tighter accuracy requirements while write time is getting longer and longer due to skyrocketing shot count. As a result, the mask cost has increased dramatically. Figure 1 shows the empirical results and forecast of shot counts for each technology node. Based on the current technologies, estimated write time of the most critical layer for 45 nm technology node is more than 20 hours. Sconce write time increases in proportion to the shot counts, both reducing shot time and suppressing shot count will soon be seriously required.

E-Beam mask writer EBM-5000$^{1)}$, which adopts 50kV variable shaped electron beam (VSB)/vector scan architecture, was developed addressing two conflicting issues;, improvement of throughput and accuracy for 45 nm technology node. For designing mask writer system, beam current density is one of the key factors to improve write time. It is estimated that write time of EBM-5000 for 45 nm technology node can be reduced to about 8 hours by increasing current density from 20A/cm^2 to 50A/cm^2. To ascertain the platform extendibility for future generation, local CD uniformity (LCDU) issue has been closely analyzed. Our error budget estimations indicate that shot noise induced CD error$^{2)}$ dependent on the number of emitted electrons is the dominant error source. The lower the resist sensitivity (higher dose), the better the LCDU. Good global CD uniformity is also achievable with the combination of stable process and the CD corrections of the EBM system. Metrology for CD and placement accuracy is another important factor to help enhance tool capability. The combination of these processes and the VSB/vector architecture with high current density is very effective to extend the tool viability to the next generation and beyond.

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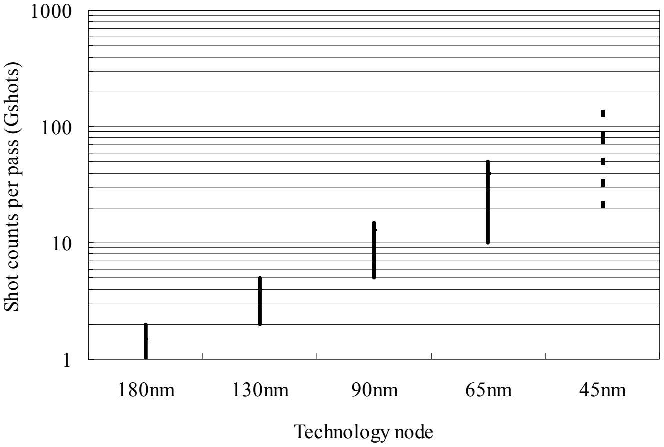

Figure 1. Shot counts by node. Empirical results for 180nm ~ 65nm node and forecast for 45nm node.

Polymer Self Assembly for Lithography Subdivision in Semiconductor Microelectronics

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The challenge of continuing to shrink dimensions of semiconductor integrated circuit elements has placed severe demands on optical lithography processes, and has created opportunities for alternative patterning approaches. We have been pursuing one such non-traditional approach – polymer self assembly - as a means for semiconductor patterning at sub-20nm dimensions.1 Self assembly is the spontaneous organization of materials into regular patterns, and under suitable conditions diblock copolymer thin films will organize into useful patterns with nanometer-scale dimensions.

We view self assembly as a useful complement to lithographic patterning processes, rather than as a lithography substitute. Polymer self assembly provides access to sub-lithographic dimensions although it patterns only a limited set of shapes and does not afford pattern registration. Combining self assembly with lithography leverages the strengths of each technique – self assembly is used to subdivide lithographic features.

We will describe the utility of lithography subdivision in the fabrication of high-performance semiconductor devices. For example, high-surface-area electrodes give passive on-chip capacitors enhanced charge storage density. As well, nanostructured floating-gate nonvolatile memory elements may have improved device scaling properties. Lithography subdivision is also effective at addressing key fabrication challenges of advanced field-effect-transistor designs. Our discussion of self assembly in these complex applications will highlight the promise and versatility of this technique as well as challenges still to be addressed.

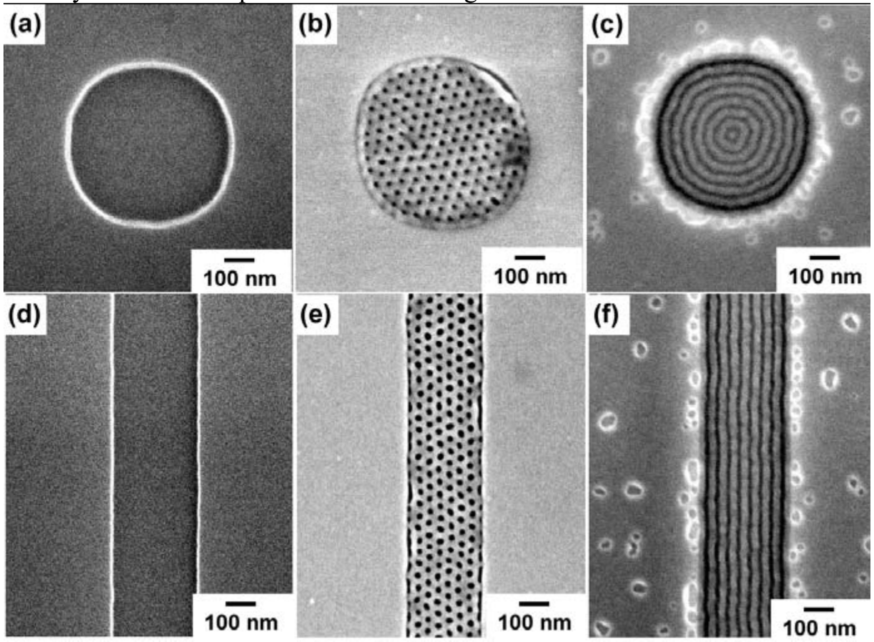

Figure 1. **Lithography subdivision by polymer self assembly**. (a), (b) Lithographically-defined shapes can be subdivided by either (b), (d) self-assembled hexagonal holes arrays, or (c), (f) equal lines and spaces.

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Will EUV lithography be limited by the performance of resists?

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We examine the imaging resolution of EUV lithography, especially taking into account the apparent limitation of chemically-amplified resists (CARs) in accurately recording the aerial image that an EUV scanner can produce. In particular, we look at the resolution of the best CARs currently available and how the acid diffusion process appears to be one of the main limiters. We evaluate methods that have been used to infer a resist resolution blur and how they correlate with imaging performance.

Our paper also compares the relative importance of the resist to other parameters affecting imaging, such as mask architecture, aberrations, and flare levels.

Finally, we explore the trade-offs between resist resolution, roughness and sensitivity, and what might be done to achieve a successful implementation of this technology.

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A New Materials Approach for 193 Immersion Lithography - Defect and Leaching Control

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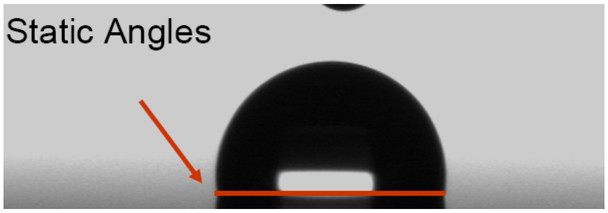
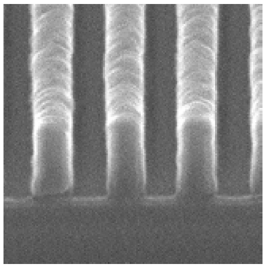
In Immersion Lithography the optical path between the lens element and the photoresist will be water. Defects have been identified as a major roadblock for the introduction of immersion lithography to real device manufacturing. Immersion specific defects can be split into two major classes – watermark & bubble defects. A number of mechanisms have been proposed as potential causes for these immersion defects. Watermark defects are potentially due to chemical interactions between water and the photoresist resulting in a termination of the acid catalyzed deprotection of the photoresist polymer. This termination can occur through leaching of components out of the resist or contaminants from the water neutralizing chemistry within the resist film. Alternatively, bubble defects are considered to be the result of bubble entrapment caused by the movement of the leading edged of the lens element across the resist surface. The formation of these bubbles causes a disruption of the optical path, resulting in superfluous diffraction and defects within the resist.

To address these immersion specific defect issues we have developed a novel additive approach for controlling the resist surface and it's interaction with water. These additives have been designed to segregate within the resist film and migrate to the resist surface. Due to the high local concentration of these additives at the resist/water interface they create a very hydrophobic surface and allow control of surface properties. Data will be presented on this novel concept, illustrating the control of leaching and resist surface hydrophobicity. The use of this new technology allows control of leaching, resist surface contact angles and immersion specific defects.



(a) Static contact angle of water on a resist surface



(b) 75nm line space pattern with resist containing additives

Lifting Lithography's Wedding Veil of Haze

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For many years, mask makers have provided low cost, high quality parts quickly to grateful wafer lithographers eager to provide the general populace with mass quantities of transistors for a price which drops by about 29% per year per device. This blissful coexistence has been disrupted recently by the prospect of a greater commitment, a marriage of sorts. Yes, I'm talking about DFM, defect free manufacturing, which threatens to bind the supply chain together like nothing else, ever. Mask makers and wafer lithographers are being forced to face their problem child we call reticle haze.

Haze is the ultimate defect: it has many causes, it is expressed in a variety of chemistries and morphologies, and it is usually visible on the reticle only after the reticle has experienced exposure in the wafer scanner. As a result, haze forces mask and wafer lithographers to work together; otherwise, like a bad marriage with kids, it will never get out of our lives and we'll blame each other for inferior product.
This paper describes reticle haze in detail: its myriad causes, techniques for characterizing it, and methods for reducing or eliminating it.

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