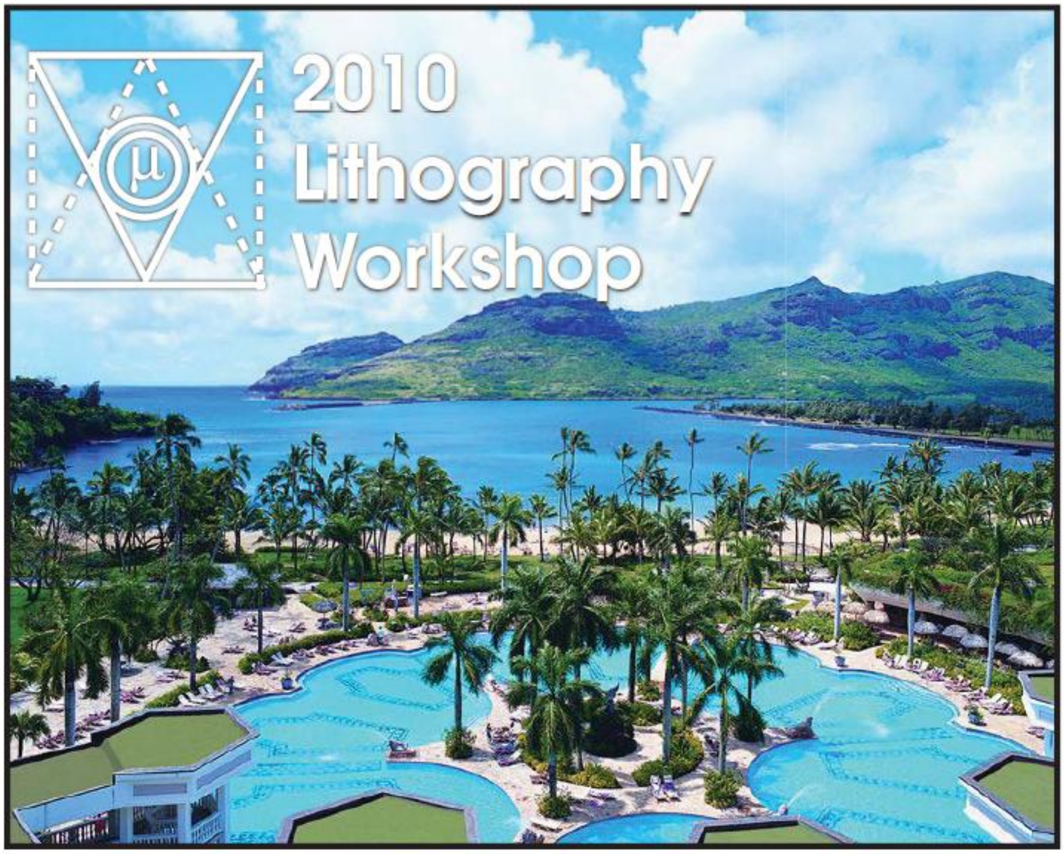


Marriott Kauai Resort in Lihue, Kauai

November 7 through November 11, 2010

President's Message
2010 Lithography Workshop

Welcome to the 20th Lithography Workshop which is being held November 7-11, 2010 at the Marriott Kauai Resort in Lihue, Kauai. With the support of its members, the Lithography Workshop has sponsored a unique program which is carefully designed to cover the latest lithography-related advancements to benefit all participants in their field of expertise. The Workshop held its first meeting in Lake Placid, New York in 1981. The 2010 Workshop is the 20th in a series of meetings that span 29 years promoting the continuing evolution of lithography. The speakers at the Workshop are selected by invitation and represent a broad range of disciplines and covering a wide array of different lithography approaches and requirements.

The Workshop is modeled to be similar to a "Gordon-Research" meeting but with the intent of addressing more immediate issues facing the lithography community within the next 3-5 years. The attendees of the Workshop share recent advances and knowledge in lithography with others in the community. The Workshop provides an environment where leading researchers from various disciplines can share their thoughts and ideas. A primary intent is to provide an arena for stimulating debate and the meeting schedule is designed to provide the attendees time for side-meetings and discussions. The Workshop has historically focused on leading-edge semiconductor applications, but has also addressed the challenging lithography needs of flat panel displays, disk drives and 3-dimensional device integration.

The Workshop format is intended to provide an atmosphere for in-depth discussions of the invited and poster papers presented. This is accomplished by providing time for questions and answers after each paper, during the poster programs and during group meetings. This year, we will continue with our very successful Poster Session to present additional, late-breaking topics of interest.

As in the past, there will be no formal proceedings, picture taking, audio or video recording of the Workshop presentations. Similarly to last year, authors will have the opportunity to voluntarily publish their presentations on the Lithography Workshop Website. The technical sessions have been scheduled for mornings and evenings, with informal meetings between attendees and authors during the afternoon.

The Executive Committee is arranging a program that we believe you will find intellectually stimulating and challenging. Putting together a meeting such as this required the contributions of many people. We are especially thankful to the Technical Program Chairpersons and the Session Chairs who have put together the program. This year, the Technical Program Chairs are Dr. Vivek Singh of Intel and Dr. Michael Fritze, currently with USC-ISI and formally with DARPA. We hope that you will avail yourself to all the sessions and functions that the organizers have planned.

The Executive Committee welcomes your comments and suggestions to better serve the lithography community.

Andrew M. Hawryluk, Ph.D.
President of the Executive Committee

"Aiming beyond the cutting edge"
At TOK, we boldly challenge ourselves to enable the "next technology, next valued product" by applying our micro fabrication technology, cultivated over the years.
Please watch as we strive for solutions beyond the cutting edge.
Semiconductor Manufacturing Field
Semiconductor Package Field
LCD Manufacturing Field
Business Segments
MEMS Manufacturing Field
Printing Plate Manufacturing Field
tok AMERICA
TOKYO OHKA KOGYO AMERICA, INC.
http://www.tok.co.jp/ *Subsidiary of TOK

ASML
Ride the wave of innovation

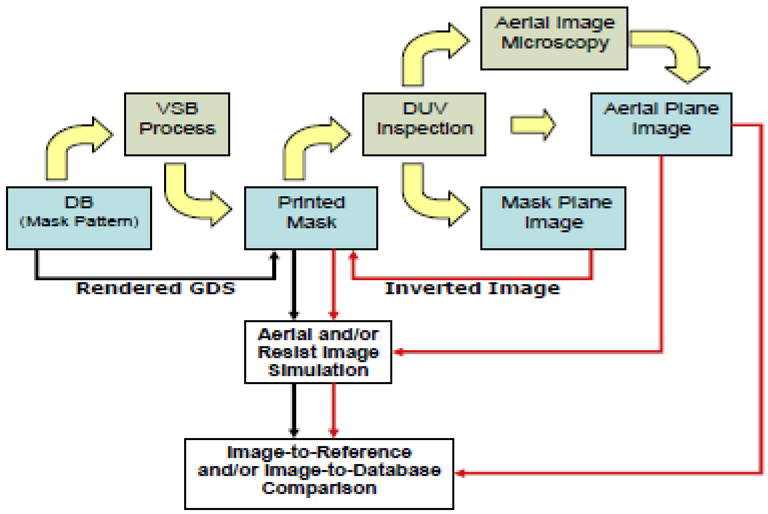
[AP Leader]
Ultratech is the technology and market leader in the advanced packaging (AP) lithography market. Our family of AP lithography systems delivers superior overlay, resolution, and side wall profile performance enabling highly-automated and cost effective manufacturing. In addition, the AP tool is particularly well suited for through silicon via applications as it features an innovative dual-side alignment (DSA) system.
www.ultratech.com
UNITY Platform
AP300
Ultratech
3050 zanker rd. san jose, ca - 95134

>> One Will Not Work Without The Other:

COMPUTATIONAL LITHOGRAPHY
COMPUTATIONAL INSPECTION, METROLOGY & REPAIR

After pioneering computational lithography and implementing it for integrated mask synthesis in production, Luminescent has successfully applied its core methods and extensive computational know-how to mask inspection, metrology and repair.

Today's masks require precision and accuracy in defect management. Luminescent has developed products that complement your expensive inspection, metrology and repair equipment, and enable them to operate at higher capability and efficiency. The results are extended use of your equipment for ILT/SMO and EUV masks, and increased ROI from mature nodes.



Gain competitive edge by using Luminescent's computational inspection, metrology and repair solutions. For more information, please contact us at luminescent@computationalinspection.com

LUMINESCENT TECHNOLOGIES

2471 East Bayshore Road
Suite 600
Palo Alto, CA 94303, USA

Phone: +1-650-433-1060
Fax: +1-650-960-3954
Web: www.luminescent.com

The Executive Committee

Andrew M. Hawryluk, President
Ultratech
ahawryluk@ultratech.com

Larry Zurbrick, Vice-President & Publications
Agilent Technologies
Larry_Zurbrick@agilent.com

John McCoy, Treasurer
john@mccoypartners.com

David Kyser, Local Arrangements Chair
Applied Materials
David_Kyser@amat.com

Ken Harrison, Secretary & Registration Chair
HG Engineering
Ken.harrison1@verizon.net

John Frankenthaler, Corporate Sponsors
F&F Associates
FandF@att.net

Kevin Cummings
ASML
Kevin.cummings@asml.com

Frank Schellenberg
franklin.schellenberg@gmail.com

Bruno La Fontaine
Cymer
Bruno_La_Fontaine@cymer.com

Juan Maldonado
Stanford University
Jrmaldo1@slac.stanford.edu

Cynthia Hanson
Space and Naval Warfare Systems Command
chanson@spawar.navy.mil

Susan Jones
Jones.susan.k@gmail.com

Keith Standiford
standifo@pacbell.net

The Sustaining Committee

Bernard Piwczyk
Jim Wiley
Carroll Fencil

Technical Program Chairs

Dr. Michael Fritze
Information Sciences Institute
University of Southern California

Dr. Vivek Singh
Intel Corporation

Technical Section Chairs

Computational Lithography	Leo Pang (Luminescent)
EUV Lithography	Bill Arnold (ASML)
Design for Manufacturing	John Sturtevant (Mentor Graphics)
Double Patterning	Lars Liebmann (IBM)
Maskless Lithography	Chris Bevis (KLA-Tencor)
Nanoimprint	S.V. Sreenivasan (Molecular Imprints Inc.)
Resists	Cliff Henderson (Georgia Tech)
Self Assembly	Paul Nealy (University of Wisconsin)
3D IC	Sitaram Arkalgud (Sematech)

2010 LITHOGRAPHY WORKSHOP

SCHEDULE OF EVENTS

Time	Sunday		Monday		Tuesday		Wednesday		Thursday	
	Program	Spouse	Program	Spouse	Program	Spouse	Program	Spouse	Program	Spouse
7:00 AM			Breakfast		Breakfast		Breakfast		Breakfast	
7:30 AM										
8:00 AM			Program	Breakfast, Puna Ct.	Program	Breakfast, Puna Ct.	Program	Breakfast, Puna Ct.	Program	Breakfast
8:30 AM										
9:00 AM										Pickup Glass, Puna
9:30 AM				Resort talk (h)						
10:00 AM				Garden Tour		Cooking Demo, Puna Ct.		Lei Class, Puna Ct.		Pickup Glass, Puna
10:30 AM										
11:00 AM										
11:30 AM										
12:00 PM										
12:30 PM										
1:00 PM			Networking and Group Activities							
1:30 PM									Program	
2:00 PM										
2:30 PM										
3:00 PM										
3:30 PM										
4:00 PM										
4:30 PM										
5:00 PM	Registration starts at 6		Reception (Posters)		Reception (Posters)					
5:30 PM							Reception			
6:00 PM	Reception, Activities Signup, Tomilyn Clark, Glass Artist: Info and Sales Table									
6:30 PM							Banquet			
7:00 PM			Program (h)	Glass Class, Hosp. Suite (h)	Program (h)	Hula Class, Hosp. Suite (h)				
7:30 PM										
8:00 PM										
8:30 PM							Panel (h)			
9:00 PM										
9:30 PM										

(h) Hospitality PM includes beer/wine, AM extend breakfast

Schedule of Presentations

Monday, November 8, 2010

	Time	Presenter	Title	Page
Session 1	8:00 – 8:25 AM	Andy Hawryluk Vivek Singh Michael Fritze	Welcome and Opening Remarks	-
	8:25 – 9:15 AM	**Tatsuhiko Higashiki** ***Plenary Speaker***	**Technical Challenges of EUVL for Semiconductor Device Production**	**14**
	9:15 – 9:40 AM	John Knickerbocker	3D Technology for Systems Applications	15
	9:40 - 10:05 AM	Lars Liebmann	Gratings of Regular Arrays and Trim Exposures for Digital Designs: ensuring cost-effective access to leading-edge technology for low-volume ASIC	16
	10:05 – 10:35 AM	BREAK		
Session 2	10:35 – 11:00 AM	Hans Meiling	EUV into production with ASML's NXE platform	18
	11:00 – 11:25 AM	Serge Tedesco	A ML2 (MAPPER) status through the « IMAGINE » industrial consortium	19
	11:25 – 11:50 AM	Lloyd Litt	SEMATECH Nanoimprint Program Update and Technology Assessment	20
	11:50 AM – 12:15 PM	Chris Progler	Pushing round pegs into square holes	21
	12:15 PM	End Session		

	5:00 – 7:00 PM	**Poster Session and Reception**		
Session 3	7:00 – 7:25 PM	Wes Hansford	3DIC Multi-Project Wafer Runs – Tezzaron MPW	23
	7:25 – 7:50 PM	Leo Pang	Computational Lithography and Computational Inspection (CLI) – Two Complementary Technologies Essential for Successful Next-Generation Lithography	24
	7:50 – 8:15 PM	Luigi Capodieci	Beyond 28nm: New Frontiers and Innovations in Design For Manufacturability at the Limits of the Scaling Roadmap	25
	8:15 – 8:40 PM	Cliff Henderson	Organic Resist Materials for sub-30 nm Patterning: Lessons Learned and Future Directions	26
	8:40 – 9:05 PM	Mike Rieger	Applying information theory to lithography flows	27
	9:05 – 9:30 PM	Vincent Wiaux	Multiple patterning... various keys for scaling	28
	9:30 PM	End Session		

Tuesday, November 9, 2010

	Time	Presenter	Title	Page
Session 4	8:00 – 8:50 AM	**Toshikazu Umatate** ***Plenary Speaker***	**Challenges for Future Lithography beyond 20 nm**	30
Session 4	8:50 – 9:15 AM	David Pan	Layout Decomposition and Routing Issues in Double Patterning Lithography	31
Session 4	9:15 – 9:40 AM	Naoya Hayashi	Nanoimprint Lithography Template Technology: Progress and Issues	32
Session 4	9:40 - 10:05 AM	Tim Crimmins	Toward high yield EUV lithography; patterned reticle and wafer defect metrology challenges and opportunities	33
	10:05 – 10:35 AM	BREAK		
Session 5	10:35 – 11:00 AM	Mark MacCord	Progress on REBL Technology for Parallel High-Throughput Electron Beam Direct Write Lithography	35
Session 5	11:00 – 11:25 AM	Simon Wong	3D SRAMs and FPGA's	36
Session 5	11:25 – 11:50 AM	Vivek Subramanian	Droplet-on-demand direct patterning of active materials: materials, modeling, and integration	37
Session 5	11:50 AM – 12:15 PM	Karl K. Berggren	Harnessing Commensuration and Local Strain to Direct Self Assembly for Lithography at the Sub-10-nm Scale	38
Session 5	12:15 – 12:40 PM	Patrick Naulleau	EUV learning at LBNL: past, present, and future	39
	12:40 PM	End Session		

	5:00 – 7:00 PM	**Poster Session and Reception**		
Session 6	7:00 – 7:25 PM	Soichi Owa	Past history of NGLs and meaning of COO analysis	41
Session 6	7:25 – 7:50 PM	Yuri Granik	Challenges in mask optimization for Optical Lithography	42
Session 6	7:50 – 8:15 PM	Walter Hu	Nanoimprinted functional polymers for biomedical and photovoltaics applications	43
Session 6	8:15 – 8:40 PM	Tom Wallow	EUV Resists Reconsidered: Optical Materials or Materials for Optics ?	44
Session 6	8:40 – 9:05 PM	Kameshwar Poolla	IMPACT Center Research in Double Patterning: flavors, performance metrics, design restrictions	45
Session 6	9:05 – 9:30 PM	Matt Nowak	Can High Density 3D Through Silicon Stacking replace lithography-driven CMOS scaling as the engine for the semiconductor industry?	46
	9:30 PM	End Session		

Schedule of Presentations

Wednesday, November 10, 2010

	Time	Presenter	Title	Page
Session 7	8:00 – 8:50 AM	**John Warlaumont** ***Plenary Speaker***	**Turning seedlings into trees: The success of consortia (SEMATECH) in bridging technology and funding gaps**	48
	8:50 – 9:15 AM	Andrezej Strojwas	Connector based designs to enable pattern controlled library for 22/20nm lithography	49
	9:15 – 9:40 AM	Andreas Wild	An ecosystem approach to double patterning: the ENIAC JU project "LENS"	50
	9:40 - 10:05 AM	Paul Nealey	Block copolymer lithography	51
	10:05 – 10:35 AM	BREAK		
Session 8	10:35 – 11:00 AM	SV Sreenivasan	Status of Jet and Flash Imprint Lithography Tool and Process Technology	53
	11:00 – 11:25 AM	Bruno LaFontaine	Performance of a Laser Produced Plasma EUV source	54
	11:25 – 11:50 AM	Yu Cao	New Applications of Computational Lithography Using Predictive Scanner Models	55
	11:50 AM – 12:15 PM	Hank Smith	Maskless Photolithography for Customization	56
	12:15 – 12:40 PM	Andrew Grenville	Imageable Oxides: New Solutions for Resist	57
	12:40 PM	End Session		

5:30 – 6:30 PM	**Reception**
6:30 – 8:15 PM	**Banquet**
8:15 – 9:30 PM	**Panel: EUV vs. Optical Extensions**
9:30 PM	End Session

Schedule of Presentations

Thursday, November 11, 2010

	Time	Presenter	Title	Page
Session 9	8:00 – 8:25 AM	Michael Thompson	Sub-millisecond Post-Exposure and Hard Bake of Chemically Amplified Photoresists.	59
	8:25 – 8:50 AM	Joy Cheng	Directed Self-Assembly for Lithography Applications	61
	8:50 – 9:15 AM	Franklin Kalk	Advanced photomasks: challenges and choices	62
	9:15 – 9:40 AM	Rudi Hendel	Extending the Limits - Embracing Restrictions:a scenario of future patterning technology.	63
	9:40 - 10:05 AM	Andrew Neureuther	Physics-Based Models for Process Awareness	64
	10:05 – 10:35 AM	BREAK		
Session 10	10:35 – 11:00 AM	Chris Bencher	An Assessment of Patterning Options for 15nm Half-Pitch	66
	11:00 – 11:25 AM	Kevin Lucas	Pattern Splitting interactions with design density and OPC complexity	67
	11:25 – 11:50 AM	Andrew Kahng	A Roadmap for DFM	68
	11:50 AM – 12:15 PM	Chenson Chen	A Decade of SOI-Based 3DIC's at MIT Lincoln Laboratory	69
	12:15 PM	End Session		

Session 11	1:40 – 2:05 PM	James Blatchford	Streamlined simulation flows for assessing design rule and patterning choices for advanced logic nodes	71
	2:05 – 2:30 PM	Juan de Pablo	A Molecular View of Block Copolymer Directed Assembly and its Application to Sub-Lithographic Patterning	72
	2:30 – 2:55 PM	Carlos Fonseca	Employing cost-effective solutions in double patterning schemes	73
	2:55 – 3:25 PM	BREAK		
Session 12	3:25 – 3:50 PM	Rick Uchida	Advanced PAG design for chemically amplified resists	75
	3:50 – 4:15 PM	John Warlaumont	Accelerating the introduction of 3D TSVs at SEMATECH	76
	4:15 – 4:40 PM	Ed Holland	Roll to roll imprint lithography for flexible electronics and structural templates.	77
	5:00 PM	End Session and Conference		

Poster Papers

Monday, November 8, 5:00 – 7:00 PM
Tuesday, November 9, 5:00 – 7:00 PM

Session 1

Presentation Schedule for Monday, November 8, 2010

Time	Presenter	Title
8:00 – 8:25 AM	Andy Hawryluk Vivek Singh Michael Fritze	Welcome and Opening Remarks
8:25 – 9:15 AM	**Tatsuhiko Higashiki** ***Plenary Speaker***	**Technical Challenges of EUVL for Semiconductor Device Production**
9:15 – 9:40 AM	John Knickerbocker	3D Technology for Systems Applications
9:40 - 10:05 AM	Lars Liebmann	Gratings of Regular Arrays and Trim Exposures for Digital Designs: ensuring cost-effective access to leading-edge technology for low-volume ASIC
10:05 – 10:35 AM	BREAK	

Technical Challenges of EUVL for Semiconductor Device Production

Tatsuhiko Higashiki,

Advanced Lithography Process Technology Dept., Toshiba Corp.,

Corporate Research & Development Center
8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan

Semiconductor manufacturing has been demanding strong pattern shrink. In a current lithography technology, a double patterning technology has started in production lines. The double patterning disadvantages are expensive process cost and opportunity cost loss due to long cycle time in production. Moreover, it is expected that EUVL appears as next-generation lithography technology.

EUVL has gone into the stage of mass-production technology from the stage of basic technology study, however still have many technical challenges for engineering. The critical issues are mask inspection and resist process. Next generation device will be mass-produced after several years later. It is difficult to accelerate EUVL technical development at one company. I think that structure mutually complemented in the world is required to realize next generation EUVL, such as mask inspections, EDA, and resist development.

I would like talk about technical challenges of EUVL for semiconductor device production.

3D Technology for Systems Applications

John Knickerbocker

Three-dimensional (3D) chip integration can provide a path to miniaturization, high bandwidth, low power, high performance and system scaling.

Integration options can leverage high bandwidth electrical and optical interconnection using stacked die, silicon packages and / or opto-electronics depending on applications. 3D enabling technology elements include: (i) through-silicon-vias (TSV) in thinned silicon wafers, (ii) fine pitch wiring, (iii) fine pitch interconnection between die, (iv) known-good die including BIST, fine pitch probes and test strategy and (v) power delivery and cooling solutions. Applications may range from miniaturization for portable electronics like image sensors and cell phones to high performance computing solutions such as servers and super computers. This presentation will discuss 3D systems, system co-design, enabling technology and challenges for 3D integration. The presentation will also report on 3D technology test vehicles, demonstrations and results.

Gratings of Regular Arrays and Trim Exposures for Digital Designs: ensuring cost-effective access to leading-edge technology for low-volume ASIC

Lars Liebmann
lliebman@us.ibm.com

As conventional optical lithography --the key enabler for semiconductor scaling-- rapidly approaches its fundamental resolution limit, the microelectronics industry is turning to double patterning and next-generation lithography solutions to maintain a path to further density scaling. While the unremitting drop in memory prices proves that these increasingly complex patterning solutions can be cost-effective for very large volume products, their economic feasibility for application-specific (ASIC) hardware customization is rapidly diminishing. Only innovative techniques for IC design and patterning that holistically address design, patterning, and fabrication challenges to reduce manufacturing cost and improve design efficiency will result in more affordable ICs across a wider range of product volumes. In this presentation we will review a DARPA sponsored IBM-CMU collaboration that explores co-optimized CMOS process extensions, design solutions, and patterning techniques with the goal of ensuring continued cost-effective access to leading-edge technology for low-volume ASIC.

This work is sponsored by the DARPA GRATE (Gratings of Regular Arraysand Trim Exposures) program under Air Force Research Laboratory (AFRL) contract FA8650-10-C-7038.

Session 2

Presentation Schedule for
Monday, November 8, 2010

Time	Presenter	Title
10:35 – 11:00 AM	Hans Meiling	EUV into production with ASML's NXE platform
11:00 – 11:25 AM	Serge Tedesco	A ML2 (MAPPER) status through the « IMAGINE » industrial consortium
11:25 – 11:50 AM	Lloyd Litt	SEMATECH Nanoimprint Program Update and Technology Assessment
11:50 AM – 12:15 PM	Chris Progler	Pushing round pegs into square holes
12:15 PM	End Session	

EUV into production with ASML's NXE platform

Hans Meiling

ASML Netherlands B.V., De Run 6501, 5504 DR Veldhoven, The Netherlands

EUVL enables continued feature shrink, delivering a cost effective solution for the manufacturing of advanced devices. Furthermore, EUV at introduction uses high k1 and thereby simplifies the imaging process. ASML brings EUVL technology into production with the introduction of the new NXE platform.

The NXE is a multi-generation TWINSCAN™ platform that builds on the experience of TWINSCAN™ technology and the two 0.25NA EUV alpha demo tools installed at research centers that are used for EUV process development. The NXE platform uses a light source with a wavelength of 13.5nm, and features reflective optics and dual stages operating in vacuum.

In this presentation we will show the key features and performance results of the NXE:3100, which is the first generation of the NXE platform. With a 0.25NA lens the NXE:3100 is aimed at EUV implementation for the 27nm half-pitch node and below. The NXE:3100 performance overview will include updates on the modules, such as source, optics, stages, and alignment - as well as system performance including overlay and imaging.

In addition we will show the latest imaging and device work performed on the EUV tools installed at the research centers, including the most recent EUV infrastructure developments. We will also present the EUV roadmap with an update of the second and third generation 0.32NA NXE tools, including off-axis illumination for high volume manufacturing of resolutions down to 16nm and a throughput of >150WpH.

A ML2 status through the « IMAGINE » industrial consortium

S.Tedesco, L. Pain

CEA – LETI, MINATEC, 17 rue des martyrs, F-38054 GRENOBLE Cedex 9, France
Phone number: (33) – (0)4 76 38 49 89 – Fax number: (33) – (0)4 76 92 50 71
E-mail address: serge.tedesco@cea.fr

Leti and Mapper have launched in July 2009 the industrial consortium "IMAGINE" focused on the development of Maskless (ML2) technology and its infrastructure.

This program provides the world's major chip manufacturers with the opportunity to assess this lithography technique in a real manufacturing environment with the following main objectives:

1. Assess the capability of MAPPER technology versus ITRS targets
2. Assess MAPPER technology against end users requirements
3. Develop and provide the necessary infrastructure
    - Process
    - Data flow
    - Proximity Effect Correction
4. Develop the applicability for 2 priority markets
    - Semiconductor Manufacturing
    - Mask Making

This worldwide unique programme on maskless has generated a lot of interest and one year later: End user's, Equipment, EDA and resist suppliers are working together toward providing to the semiconductor industry a ML2 lithography solution.

This presentation will give an update of the latest results achieved inside "IMAGINE". A first status on the possibilities of this solution will be drawn. A discussion on the potential ML2 insertion point into industry pilot lines will be engaged to conclude this work.

SEMATECH Nanoimprint Program Update and Technology Assessment

Lloyd C. Litt[a,b] and Matt Malloy[a]
[a]SEMATECH, 257 Fuller Road, Albany, NY USA 12203
[b]GlobalFoundries, Sunnyvale, CA USA 94085

Nanoimprint Lithography Session
Lithography Workshop, November 7-11, 2010

SEMATECH's investigation of nanoimprint was initiated in late 2008 with the installation of the first Imprio300 from Molecular Imprints. The primary program focus includes study of key technology issues of nanoimprint application to semiconductor manufacturing and system performance characterization.

Nanoimprint has shown promising results, especially in resolution and pattern fidelity, provided a good quality template can be produced. Sub-30nm HP features with low LWR have been printed over full 26x32mm fields. Mix and match overlay below 17nm mean+3s has been demonstrated over several 300mm wafers which is 1/2 of the initial system specification. While this performance is not yet at the requirements for 22nm node manufacturing, it is an important step toward the final goal and was accomplished primarily by improvements in template image placement error reduction. Defectivity requires significant development to reach the levels required for semiconductor production. Particle contamination issues are a concern due to the contact nature of the technology and is currently an area of specific attention.

A status report on the Imprio300 tool performance will be presented including the latest overlay and defectivity results as well as tool stability, capability, and SPC data .Updates on other ongoing nanoimprint projects at SEMATECH will also be presented.

Keywords: Nanoimprint, NIL, Imprio300, Molecular Imprints, lithography

Brief CV:

Lloyd C. Litt received his bachelor's and master's degrees in Imaging and Photographic Science from Rochester Institute of Technology. He has worked in semiconductor lithography development since 1985 at companies including IBM, Motorola/Freescale, and AMD/GLOBALFOUNDRIES. Lloyd is currently the Alternative Lithography Program Manager at SEMATECH in Albany,NY, and is an assignee from GLOBALFOUNDRIES.

lloyd.litt@sematech.org

Pushing Round Pegs Into Square Holes

Christopher Progler
Photronics Inc.

Directly injecting wafer lithography information into the mask production process in order to extend technology, improve yield and reduce costs for both sides has been a common but often elusive goal for many years. The most notable success on the mask process side comes from using an aerial image based microscope (i.e., AIMS) to analyze defects on the photomask using nominal lithography printing conditions. In the other direction, we have seen a productive flow of real information from the mask manufacturing side into the wafer printing process For example, densely mapped mask inspection data is now providing a feed forward into lithography scanner dose correction algorithms to improve wafer level CD control. As we also know, mask making processes are indirectly captured in the calibration of OPC models for improving the fidelity of wafer prints and embedded wafer simulation is working into mask equipment on a more routine basis.

In this talk, we will review how technology and information crosstalk between mask and wafer manufacturing occurs on direct and indirect levels. We will look forward at double patterning, source-mask optimization and EUV to assess how this trend is likely to continue and grow in importance. We will also consider ways in which the optical properties of masks will drive greater uncertainty in mask specifications forcing the need for an even tighter interlock between mask and wafer processing.

Session 3

Presentation Schedule for
Monday, November 8, 2010

Time	Presenter	Title
7:00 – 7:25 PM	Wes Hansford	3DIC Multi-Project Wafer Runs – Tezzaron MPW
7:25 – 7:50 PM	Leo Pang	Computational Lithography and Computational Inspection (CLI) – Two Complementary Technologies Essential for Successful Next-Generation Lithography
7:50 – 8:15 PM	Luigi Capodieci	Beyond 28nm: New Frontiers and Innovations in Design For Manufacturability at the Limits of the Scaling Roadmap
8:15 – 8:40 PM	Cliff Henderson	Organic Resist Materials for sub-30 nm Patterning: Lessons Learned and Future Directions
8:40 – 9:05 PM	Mike Rieger	Applying information theory to lithography flows
9:05 – 9:30 PM	Vincent Wiaux	Multiple patterning... various keys for scaling
9:30 PM	End Session	

3DIC Multi-Project Wafer Runs – Tezzaron MPW

Wes Hansford
(USC-ISI MOSIS Service)

It has recently become practical to implement 3DIC systems using a mix of CMOS technology integrated circuits into a multi-tier structure that integrates analog, RF and digital systems onto a single die foot-print. The initial efforts by DARPA and the High Energy Physics (HEP) community has identified a commercial path for implementing shared 3DIC Multi-Project Wafer (MPW) runs using a 3DIC process that is supported by Tezzaron Semiconductor. The MOSIS Service has developed a business relationship with Tezzaron to provide MPW runs using a 130 nm CMOS technology from Global Foundries in the near term with future offerings to include on-shore CMOS foundries. These early MPW runs will permit two tier designs with both tiers being fabricated at the same CMOS foundry. This will permit 3D stacking of CMOS designs optimized for both analog and digital systems. At some point in the future more tiers will be permitted and there will be standard memory die that can be added to the 3D stack along with other technologies. The Tezzaron 3DIC technology utilizes "super-via" to provide between tier interconnect at many points within the area of the active chip area.

After the top wafer of the two tier stack has been thinned to reveal the tips of the super-via, a pattern of copper bond structures can be fabricated on the thinned wafer to permit stacking another wafer on top to make a three tier structure. This process can be repeated to stack many die to produce an equivalent of another node of circuit density without requiring another lithography upgrade to a smaller feature size. This technique is not limited to standard CMOS technology.

This 3DIC technology MPW offering is a significant step toward being able to implement complex high density integrated systems without incurring the high cost associated with more advanced smaller feature size technologies. Also, there will not be a need to wait for the next technology node in order to place the next generation system on a desired chip footprint. The strategy used for this offering is to fabricate wafers up to the metal 4 level and then cap the metal with silicon nitride to permit subsequent fabrication of TSV's and several upper level metal layers at a separate fabrication facility. This strategy of using a modified via-middle process that is compatible with essentially any CMOS (or SiGe) commercial foundry process opens many opportunities for technology diversity in 3DIC's without imposing TSV technology upon commercial foundries.

Computational Lithography and Computational Inspection (CLI) – Two Complementary Technologies Essential for Successful Next-Generation Lithography

Linyong Pang, Danping Peng, Peter Hu, Dongxue Chen, Lin He, Chris Clifford, Ying Li, Vikram Tolani, Noel Corcoran, Grace Dai
Luminescent Technologies, Inc. 2471 East Bayshore Road, Suite 600,
Palo Alto, CA 94303, USA

Lithography has evolved rapidly over the last several years, but the upcoming 20nm and 16 nm technology nodes, which may also rely on new EUV source and scanner, will present an even greater challenge than ever. This challenge is answered by two new critical enabling lithography technologies - computational lithography (i.e., Inverse Lithography Technology (ILT) and Source Mask Optimization (SMO)), and computational inspection. Mask patterns (including Sub-Resolution Assistance Features, or SRAFs) generated by ILT and SMO become essential for production at the 20nm node. However, their use results in significantly increased mask complexity, making mask defect disposition more difficult than ever. Computational Lithography and Inspection (CLI) have broad applications in mask inspection, metrology, review, and repair, and provide additional information to assist the operator in making accurate and efficient decisions on defect disposition. Once EUV lithography is introduced, OPC may become simpler but mask defect detection and disposition will become a critical issue. Computational Lithography will be still needed, but accurate modeling and fast simulation will be more important than ever. Since actinic EUV mask inspection and AIMS™ won't be available for the next couple of years, CLI will play a significant rule in filling the technology gap. For example, fast mask defect simulation for both absorber and multilayer, defect printability prediction by using DUV inspection images, and mask defect compensation for multilayer defects will all require CLI techniques. In this paper, applications of CLI are showcased in the areas of litho and design rule development, full chip correction, mask inspection, review, metrology, and review, and CLI techniques for EUV are presented for mask defect simulation, printability prediction, and compensation in repair.

Beyond 28nm: New Frontiers and Innovations in Design For Manufacturability at the Limits of the Scaling Roadmap

Luigi Capodieci, Ph.D.
R&D Fellow, Director DFM/CAD – GLOBALFOUNDRIES

The introduction of 28nm high-volume production for IC semiconductor devices will usher the era of "extreme low-k1" manufacturing, i.e. the unprecedented situation in the long history of the silicon technology roadmap, where computationally intensive (and EDA-driven) Design-Technology Co-Optimization will become the key enabler to a product success in terms of yield, time-to-market and profitability.

This talk will provide a review and technical analysis of the methodological innovations in Design Enablement flows which are being introduced for early production at 28nm, particularly advanced DFM physical verification and DFM-aware router implementations. Rule-based, model-based and the newly released pattern-matching based hybrid verification, pioneered, industry-first, at GLOBALFOUNDRIES are prominent examples of these new enablement flows.

DFM methodologies are complemented by a set of novel foundry-based flows identified as Design-Enabled Manufacturing (DEM). While DFM provides process awareness into the design cycle through accurately calibrated models and verification flows (DFM sign-off), DEM enables manufacturing/design co-optimization, using automated physical design analysis and characterization, which in turn drive process optimization, fine-tuned to specific customer product designs.

The presentation will conclude with a preview of the "variability-challenge" intrinsic in the 20nm node and with an anticipation of the innovative EDA solutions which are currently being developed in the new Foundry-supported *collaborative* eco-system.

Organic Resist Materials for sub-30 nm Patterning: Lessons Learned and Future Directions

Clifford L. Henderson
School of Chemical & Biomolecular Engineering
Georgia Institute of Technology

There are a host of fundamental issues that control the performance of organic and polymeric resist materials, and which limit their performance as attempts are made to use them for the high volume production of sub-30 nm features. This talk will highlight and summarize some of the most important lessons learned over the last few years in our group, both in terms of fundamental effects that are important in controlling the lithographic performance of organic resists and some possible new directions for organic resists that promise to allow for materials with high sensitivities, low edge roughness, and resolution capabilities below 20 nm. First, the fundamental aspects of resist pattern collapse will be discussed and both experimental and modeling data will be shown that highlight the challenges organic materials face in attempting to meet sub-30 nm patterning requirements. The results of studies on novel reactive rinse and adhesion control strategies will then be discussed in an attempt to show what might be possible in terms of resolving some of the pattern collapse issues discussed earlier. Finally, a brief review of some promising new resist architectures and chemistries will be presented in an attempt to show how new thinking about organic resist design may also offer some hope for the future.

Applying information theory to lithography flows

Mike Rieger

Design states of an integrated circuit undergo several transformations on the path from conception to pattern transfer to Silicon. The information content -- number of binary bits or equivalent – needed to represent a design along the way inexorably grows as the design moves closer to manufacturing. In this talk we apply information theory to estimate the minimum quantities of information (bits) needed to fully represent the states of a design at key stages, factoring in the effects of noise sources. These estimates will be compared to actual and forecast database sizes at several design states, including chip layouts, mask layouts, mask writer and direct-wafer writer primitive data streams. This work is intended to help identify potential information flow inefficiencies, and to provide theoretical benchmarks for optimum data representations at key pattern-transfer stages.

Multiple patterning... various keys for scaling

Vincent Wiaux
Vincent.Wiaux@imec.be

Extending the use of 193 immersion lithography requires combining innovative scaling solutions. Both for single and multiple patterning, smaller layouts area will need integrated design and process options. Double and multiple patterning refer to a variety of processes envisioned as potential scaling enablers. However each of those processes requires some compliance from the target design, as well as suited design decomposition. At each technology node, a cost-effective and optimum patterning flow will need to be selected depending on the layer and the application, by combining selected techniques.

We review in this paper various multiple patterning techniques and we illustrate their feasibility. Litho-Process-Litho-Etch (LPLE) processes, cost effective alternatives to Litho-Etch-Litho-Etch (LELE), have been demonstrated experimentally at 32m hp and 26hp for the line patterning of unidirectional as well as more ‘random’ layouts. LELE process has been used for the trench patterning of random logic layout at 32nm hp. Split, design, and process requirements are discussed to ensure improved density and robust stitching through process window variations. Source-Mask-Optimization with freefrom illumination has been combined with LELE for the patterning of Contact and Metal layers of 22nm node SRAM. Other techniques will also be discussed, amongst which how multiple patterning can further improve the resolution limit towards 1Xnm hp.

Session 4

Presentation Schedule for
Tuesday, November 9, 2010

Time	Presenter	Title
8:00 – 8:50 AM	**Toshikazu Umatate** ***Plenary Speaker***	**Challenges for Future Lithography beyond 20 nm**
8:50 – 9:15 AM	David Pan	Layout Decomposition and Routing Issues in Double Patterning Lithography
9:15 – 9:40 AM	Naoya Hayashi	Nanoimprint Lithography Template Technology: Progress and Issues
9:40 - 10:05 AM	Tim Crimmins	Toward high yield EUV lithography; patterned reticle and wafer defect metrology challenges and opportunities
10:05 – 10:35 AM	BREAK	

Challenges for Future Lithography beyond 20nm

Toshikazu Umatate
Nikon Corporation

The semiconductor Industry has been making continuous and rapid growth over the past 30 years. One of the drivers for this growth has been the industry's ability to scale along Moore's law, effectively doubling transistor density every 2 years and lowering the cost per transistor. Optical Lithography has been the key technology engine that has supported and enabled this scaling. The industry has used lenses with ever increasing NAs, shorter wavelengths and smaller k_1-factors to realize smaller feature sizes and better imaging capability.

Currently, optical lithography concerns itself with ArF extensions using multiple exposure processing, EUV lithography and other "next generation lithography" options that target 20nm half-pitch and beyond. These developments have many challenges that include a much wider technology area that has been previously examined. Hence, this technology requires substantial development at the extremes of our knowledge of photolithographic imaging. This results in longer development times and larger R&D investments as compared to previous generations. Consequently, selection of the probable future technology is intertwined with cost and timing issues when considering the wider business consequences.

This talk will analyze the current status and challenges of optical lithography as the industry proceeds to 20nm and beyond. Additionally, the strategy of future lithography will be discussed and prospects for the future will be proposed.

Layout Decomposition and Routing Issues in Double Patterning Lithography

David Pan
Department of Electrical and Computer Engineering
The University of Texas at Austin, TX 78712

For 22nm node and below, lithography is facing tremendous challenges and double patterning lithography (DPL) is considered the most likely candidate for 22nm/16nm nodes. The concept of double patterning may be extended to triple or even quadruple patterning as shown by Intel. There are some new DFM challenges related with DPL, including layout decomposability, stitch minimization, overlay control/compensation, balanced density, etc. This talk will present some recent results on DPL layout decomposition and DPL-aware routing. In particular, a novel multi-objective layout decomposition framework is developed, which can simultaneously minimize the number of stitches, self-compensate the overlay variations, and balance the double patterning density [ASPDAC 2010]. The DPL effect shall be considered earlier on during physical design, in particular lower metal layer (M1, M2) routing due to complicated structures, insertion of redundant vias, and so on. We will present several DPL aware routing techniques which work together with layout decomposition to improve the overall quality of results [ICCAD'08, DAC'09, ICCAD'10].

Biography

David Z. Pan is currently an Associate Professor at the Department of Electrical and Computer Engineering, University of Texas at Austin. He received his Ph.D. in computer science (with honor) from UCLA in 2000. He was a Research Staff Member at IBM T. J. Watson Research Center from 2000 to 2003. His research is mainly focused on design for manufacturing/reliability, nanometer physical design, intersection of physical and system-level co-design, and CAD for emerging technologies. He holds 8 U.S. patents and has published over 120 technical papers in premier journals and international conferences. He has served as an Associate Editor for *IEEE Transactions on CAD*, *IEEE Transactions on VLSI*, *IEEE Transactions on CAS-I*, *IEEE Transactions on CAS-II*, *IEEE CAS Society Newsletter*, and *Journal of Computer Science and Technology*. He has served as the IEEE CANDE Committee Chair, ACM/SIGDA Physical Design Technical Committee Chair, committee member of major VLSI/CAD conferences, including ACISC (Program/General Chair), ASPDAC (Topic Chair), DAC, DATE, ICCAD, GLSVLSI (Publicity Chair), ISCAS (CAD Track Chair), ISLPED (Exhibits Chair), ISPD (Program/General Chair), ISQED (Topic Chair), SLIP (Publication Chair), VLSI-DAT (EDA Chair). He is a member of the *International Technology Roadmap for Semiconductor (*ITRS*)*. He is a Technical Advisory Board member of Pyxis Technology, Inc.

He has received a number of awards for his research contributions and professional services, including ACM/SIGDA Outstanding New Faculty Award, NSF CAREER Award, UCLA Engineering Distinguished Young Alumnus Award, IBM Faculty Award (three times), SRC Inventor Recognition Award (three times), ACM Recognition of Service Award (twice), Best Paper Award at ASPDAC 2010, Best IP Award at DATE 2010, Best Student Paper Award at ICICDT 2009, Best Paper In Session Award at SRC Techcon (twice), ISPD 2007 Global Routing Contest Awards, eASIC Placement Contest Grand Prize (2009), and a number of Best Paper Award Nominations (at ASPDAC, DAC, ICCAD, ISPD). He is an IEEE CAS Society Distinguished Lecturer for 2008–2009.

Nanoimprint Lithography Template Technology: Progress and Issues

Naoya Hayashi
DNP
Nanoimprint Lithography Session
Lithography Workshop, November 7-11, 2010

Nanoimprint lithography is one of the candidates of lithography towards 2xnm and beyond. Template fabrication is one of the most critical technology challenges to realize nanoimprint lithography for semiconductor high volume manufacturing option. In this presentation, update of development status of template infrastructure and issues associated with templates for high volume manufacturing will be presented.

Biographical Information for Naoya Hayashi:
Naoya Hayashi received his BS degree in applied chemistry, and MS degree in electric chemistry from Tokyo Institute of Technology, Tokyo, Japan. He joined Dai Nippon Printing Co.,ltd. in 1977, and he has been involved in photomask fabrication technology development including E-Beam exposure systems and processes for more than 28 years in DNP. Since 1992, he has been responsible for research & development of advanced photomask technologies including OPC'ed and phase-shifting mask. He has been the General Manager of Electronic Device Laboratory since 2002, and a Senior Researcher since 2005. He became the first Research Fellow of DNP in June, 2007.

Toward high yield EUV lithography; patterned reticle and wafer defect metrology challenges and opportunities

Timothy F. Crimmins

Economical implementation of EUV lithography will require deployment at high yields. Both blank and “hard” (absorber pattern) mask defects will need to be detected and eliminated from the mask manufacturing process, but the delivery of defect-free masks to the fab is only the first step in assuring high yield printing. “Soft” defects, such as drop on particles, will need to be detected and dispositioned as part of ongoing reticle requalification efforts, requiring in situ and stand alone patterned mask inspection in conjunction with AIMS. Wafer inspection metrology capable of detecting minimum pitch printed pattern defects will play a critical role in providing development feedback and excursion control.

Focusing on EUV mask and exposed-wafer pattern metrology in the fab environment, the present work articulates the technology scheme options for contamination monitoring. Sensitivity requirements and system challenges are presented, including the role of “print checks” by wafer inspection which is critically examined from an economical and technical perspective. An overall conclusion drawn is that four technologies are both a high technical risk and required for economical, high yield printing: In situ and stand alone mask inspection, AIMS and patterned wafer inspection.

Session 5

Presentation Schedule for
Tuesday, November 9, 2010

Time	Presenter	Title
10:35 – 11:00 AM	Mark McCord	Progress on REBL Technology for Parallel High-Throughput Electron Beam Direct Write Lithography
11:00 – 11:25 AM	Simon Wong	3D SRAMs and FPGA's
11:25 – 11:50 AM	Vivek Subramanian	Droplet-on-demand direct patterning of active materials: materials, modeling, and integration
11:50 AM – 12:15 PM	Karl K. Berggren	Harnessing Commensuration and Local Strain to Direct Self Assembly for Lithography at the Sub-10-nm Scale
12:15 – 12:40 PM	Patrick Naulleau	EUV learning at LBNL: past, present, and future
12:40 PM	End Session	

Progress on REBL Technology for Parallel High-Throughput Electron Beam Direct Write Lithography

Mark McCord, Paul Petric, Chris Bevis, Allen Carroll, Alan Brodie, Upendra Ummenthala, Luca Grella, and Regina Freed
KLA-Tencor, One Technology Drive, Milpitas, CA 95035

REBL (Reflective Electron Beam Lithography) is a program for the development of a novel approach for high-throughput maskless lithography. The program at KLA-Tencor is funded under the DARPA Maskless Nanowriter Program. A DPG (digital pattern generator) chip containing 1 million reflective pixels that can be turned on or off is used to project a pattern onto the wafer. The DARPA program is targeting 5 to 7 wafers per hour at the 45 nm node, and we will describe extensions to both increase the throughput as well as extend the system to the 32 nm node and beyond.

REBL utilizes several novel technologies to generate and expose lithographic patterns at throughputs that could make ebeam maskless lithography feasible for manufacturing. The DPG will incorporate CMOS on-chip circuitry in order to provide the extremely high data rates without excessive interconnect. The exposure strategy uses a TDI (time delay integration) technique of scrolling data across the DPG in synchronicity with the stage motion, which provides both redundancy for defective pixels as well gray-level exposure control for proximity effect correction and sub-pixel edge placement. The stage will be a rotary mag-lev design that can hold and expose up to 6 wafers at a time. Wafer registration will be based on non-actinic optical metrology of marks placed on the wafers as well as on spokes between wafers.

The talk will focus on three specific areas of REBL technology. First, we have developed a new column technology based on a wien filter to separate the illumination and projection beams. Previously our column design used a magnetic prism which provided proof of concept but was too large for a practical system. The new column design is much smaller, and has better performance both in resolution and throughput. Second, we will give an update on our development of the DPG chip that modulates the beam into a million individual pixels. We have developed a microlens approach that is being fabricated on top of a CMOS driver chip. The microlens array eliminates crosstalk between adjacent pixels, maximizes contrast between on and off states, and provides matching of the NA between the DPG reflector and the projection optics. Currently we have successfully demonstrated lenslets on a plain silicon substrate, and are in the final stages of fabricating lenslets on top of active CMOS circuitry. Third, we will show our latest printing results which include lines and spaces in both PMMA and CA resists. The prints were done using our array of 1 million passive lenslets in a quasi-static mode.

3D SRAM and FPGA

Simon Wong
Stanford University

We illustrate the performance advantages of 3D integrated circuits with two specific examples, 3D-SRAM and 3D-FPGA. Through strategic modification of the architectures to take advantage of 3D, significant improvement in speed and reduction in power consumption can be achieved. We show that a 3D-SRAM can achieve about 5 times reduction in power-delay over conventional 2D-SRAM,.and a monolithically stacked 3D-FPGA can achieve about 2.5 times reduction in critical path delay and 2.9 times reduction in dynamic power consumption over a conventional 2D-FPGA

Droplet-on-demand direct patterning of active materials: materials, modeling, and integration

Vivek Subramanian
Department of Electrical Engineering and Computer Sciences
University of California, Berkeley

In recent years, there has been significant interest in the applications of printed electronics in the realization of a range of low-cost, large area, flexible electronic systems. Printing of active circuitry is expected to enable a dramatic reduction in the overall cost of these systems, allowing for integration of electronic barcodes and product quality detection systems into consumer goods. Printing techniques that have been considered range from high-speed commercial gravure printing through ultra-scaled inkjet printing. While many of the printing techniques under consideration have evolved from techniques already widely deployed in graphic arts applications, the requirements for printed electronics are in many ways dramatically different from those that exist for conventional graphic arts.

In this talk, I will review the challenges for realizing printed electronics. Specifically, I will discuss the challenges associated with utilizing printing to realize printed semiconductor-based circuits, including analyses of layer-to-layer registration, line-edge roughness, thickness control, surface energy control, and general pattern fidelity issues. Additionally, I will overview the state of the art in printed electronic materials. I will review our work on developing materials, processes, devices, and circuit architectures for printed electronic systems, and will discuss the problems that remain to be solved and opportunities that exist to make printed electronics a success.

Harnessing Commensuration and Local Strain to Direct Self Assembly for Lithography at the Sub-10-nm Scale

Karl K. Berggren

Self-assembly can be used as an lithographic accelerator to increase feature density, reduce write times, and permit complex patterns to be formed. The materials used for this self-assembly include block copolymers, quantum dots, as well as conventional electron-beam resists. However, accurate control of the template features can require patterns to be formed with ultra-narrow feature dimensions. I will present a variety of lithographic methods based on electron and helium-ion beams by which sub-10-nm features can be achieved for this. We will present methods of robust patterning of templates at the sub-10- and even sub-5-nm length scale. We will present methods by which this ultra narrow patterning can be used to control feature period and orientation using sparse patterns that are not always intuitively connected to the original pattern. Finally, we will present some recent results showing how surface-tension effects at the nanoscale can be taken advantage of to produce complex designs by using high-aspect-ratio pillars that then collapse during drying. These effects might be useful in a variety of lithographic scenarios.

EUV learning at LBNL: past, present, and future

Patrick P. Naulleau
Center for X-ray Optics, Lawrence Berkeley National Laboratory, Berkeley CA

As Extreme ultraviolet lithography (EUVL) progresses in the commercialization phase, industry activities are being focused on near term concerns. The question of the extendibility of EUVL, however, remains crucial given the magnitude of the investments yet required to make EUVL a reality. The questions of extendibility are best addressed using advanced research tools such as the SEMATECH Berkeley microfield exposure tool (MET) and actinic inspection tool (AIT). Utilizing Lawrence Berkeley National Laboratory's Advanced Light Source facility as the light source, these tools benefit from the unique properties of synchrotron light enabling research at nodes generations ahead of what is possible with commercial tools.

The MET for example uses extremely bright undulator radiation to enable a lossless fully programmable coherence illuminator. Using such a system, resolution enhancing illuminations achieving k1 factors of 0.25 can readily be attained. Given the MET numerical aperture of 0.3, this translates to an ultimate resolution capability of 12 nm.

A potential problem for advanced resist testing is also the availability of suitable masks. The MET illumination system can also address this concern through the implementation of a process we refer to as pseudo phase shift mask which allows a conventional binary amplitude mask to behave as a chromeless phase shift mask enabling pitch splitting. With this process, 12-nm resolution can be achieved with 24-nm coded features on the mask. Given the MET magnification of 5x, this translates to 120-nm features on the mask.

In addition to source and resists, defect free masks remain a significant concern for EUVL. Making progress in the near term and providing learning for the long term requires advanced metrology capabilities. Given the resonant reflective structure of EUVL masks, the use of actinic metrology is crucial. The use of synchrotron radiation enables metrology systems to be based on low-cost high performance diffractive optics. The AIT is an example of such a tool. The small size and low cost of the diffractive optics used in the AIT allow for a turret type of design whereby one can easily switch between aerial image modeling mode and higher resolution microcopy mode providing for simultaneously both lithographically relevant printability studies and defect characterization studies.

In this presentation learning from the MET and AIT systems will be used to present an assessment of critical challenges facing EUVL in the resist and mask areas with a particular focus on future nodes. The development of next generation advanced research tools addressing the learning needs out to the 8-nm node will also be presented.

Session 6

Presentation Schedule for
Tuesday, November 9, 2010

Time	Presenter	Title
7:00 – 7:25 PM	Soichi Owa	Past history of NGLs and meaning of COO analysis
7:25 – 7:50 PM	Yuri Granik	Challenges in mask optimization for Optical Lithography
7:50 – 8:15 PM	Walter Hu	Nanoimprinted functional polymers for biomedical and photovoltaics applications
8:15 – 8:40 PM	Tom Wallow	EUV Resists Reconsidered: Optical Materials or Materials for Optics ?
8:40 – 9:05 PM	Kameshwar Poolla	IMPACT Center Research in Double Patterning: flavors, performance metrics, design restrictions
9:05 – 9:30 PM	Matt Nowak	Can High Density 3D Through Silicon Stacking replace lithography-driven CMOS scaling as the engine for the semiconductor industry?
9:30 PM	End Session	

History of NGLs and implications of COO analysis

Soichi Owa
Nikon Corporation
201-9 Miizugahara, Kumagaya, Saitama, Japan 360-0844
owa@nikongw.nikon.co.jp

In 1998, the first full field ArF (193 nm) scanner was constructed and shipped to the field. Since then, 193 nm lithography has been the workhorse of high volume manufacturing for cutting edge semiconductor devices.

In the pursuit of the next lithography solution to follow 193 nm, several technology candidates have been proposed, and those were classified as 'Next generation lithography (NGL)' techniques. X-ray projection (XPL), Ion projection (IPL), Electron projection (EPL) and Extreme ultraviolet (EUVL) were the four initial NGL solutions considered in early 1998, with F2 (157 nm) lithography entering into the NGL competition later in 1998-99.

In my presentation, I plan to review and discuss how lithography technology developments have evolved over time. This discussion will be based on the viewpoint of a development member of the Nikon F2 and water-based immersion lithography programs. While F2 turned out to be a fruitless and disappointing NGL technology, water-based immersion has been very extremely successful and is currently being used worldwide in high volume manufacturing.

In addition to the previously mentioned NGLs, EB direct write (EBDW), Nano imprint, Electron proximity (LEEPLE), and High index immersion (HIL) have since entered in the competition, all aiming to be the successor of water-based immersion.

Some of these NGL techniques are no longer under active development. Currently, IPL, XPL, EPL, F2, LEEPEL papers do not appear (or are extremely limited) at the SPIE Advanced lithography conference. Whereas EUVL, EBDW, and Nano imprint are all being actively discussed and compared with double/multiple patterning technologies, which are techniques for extending water-based immersion.

When we compare NGLs, Cost of Ownership (COO) is frequently analyzed. This is the unit cost necessary for the lithography tool owner to produce a wafer using the proposed technology. It is generally felt that the technology with the lowest COO is the best and most promising among the possible candidates. Therefore, NGL developers are very focused on efforts to reduce COO values.

However, when we look back at historical COO data from today's viewpoint, we find interesting and somewhat embarrassing results. For example, in the case of 1999 data - IPL had the best (lowest) COO, XPL came in second, EPL was ranked third, F2 was fourth, and EUVL ranked fifth. Of those five candidates, only the 'worst' ranked COO technology - EUVL survived; whereas the other 'better' COO technologies are no longer active.

Further, when we consider recent COO analysis, 'Spacer-based double patterning (SDPL)' was determined to have the highest (worst) COO, while high index immersion (HIL) had the lowest (best) COO. However, it is SDPL that has been successfully adopted for NAND flash production, while HIL development was terminated.

In my presentation, I plan to study more historical COO data of various NGL solutions and discuss the associated implications.

Challenges in mask optimization for Optical Lithography

Yuri Granik
Mentor Graphics Corporation

We scrutinize the challenges of Litho Mask Optimization (aka Inverse Lithography) problems that materialize during the development of a new line of products from Mentor Graphics.

PIXBar software rigorously states and solves mask optimization problems using state of the art mathematical and computational frameworks.

We discuss challenges in stating the objective function, and in dealing with the huge size of this optimization problem. Non-convexity and ill-conditioning have to be overcome to reliably deliver accurate optimal mask configurations. Mask manufacturing considerations complicate solutions, and, along with limits on the reticle shot count, represent obstacles to broad acceptance for all design layers. We demonstrate the capabilities of PIXBar in optimizing contact and low metal layers for the best process window and optimal process variability bands.

Nanoimprinted Functional Polymers for Biomedical and Photovoltaics Applications

Walter Hu
University of Texas at Dallas
Nanoimprint Lithography Session
Lithography Workshop, November 7-11, 2010

Recently, functional polymeric nanostructures have shown strong potential for several areas of applications in medicine and energy. In this talk, I will present our recent work on applying nanoimprint lithography to fabricate a variety of “top-down” nanostructures in functional polymers with well controlled geometry and uniformity. Using these nanostructures as a platform, we study structural-property correlations, bio-abio interfaces/interactions, and their impact on various applications in nanomedicine, photovoltaics, and tissue engineering. For example, nanoimprint lithography is tailored to fabricate shape-specific and uniform nanoparticles (nanorods, nano-worm, nano-disc) for targeted drug delivery, to make nanostructured topography for controlled cell growth, and to build micro-cage devices with nano-slits towards encapsulated islet therapy. Similar nanoimprint process is applied to define optimal nano-morphology of photovoltaic heterojunction and to induce favorable 3D chain alignment in polymer nanostructures. For these applications, the imprinted nanostructures have shown positive impacts that are impossible or difficult to achieve by conventional methods.

Biography: Walter Hu received the B.S. degree from Peking University, Beijing, China, in 1999, and the Ph.D. degree from the University of Notre Dame, Notre Dame, IN, in 2004. Then, he spent a year as a post-doctoral research fellow at the Department of Electrical Engineering, University of Michigan, Ann Arbor, MI. In September 2005, he joined the Department of Electrical Engineering of the University of Texas at Dallas as an assistant professor. His research has been focused on lithography, nanofabrication, and applications in semiconductors, medical and energy areas. He has published about 30 peer-reviewed journal articles, 3 patent applications, and more than 50 conference abstracts/papers. Dr. Hu’s research has been funded by National Science Foundation (NSF CAREER award), National Institute of Health, Texas Instruments, U.S. Air Force, U.S. Army, Texas Higher Education Coordinating Board, Moncrief Foundation, Texas Med, and FUSION. He is a member of Sigma Xi, IEEE, AVS, MRS, ACS, and SPIE.

EUV Resists Reconsidered: Optical Materials or Materials for Optics?

Tom Wallow
GlobalFoundries, Sunnyvale CA

A notable and curious transformation has recently occurred in discussions of EUV resist development. In previous years, conferences and publications have predominantly framed fundamental EUV resist issues as optical film issues: image blur; shot noise limits; inherent resolution-LER-sensitivity tradeoffs, etc. More recently, however, discussion has shifted toward materials and process: new resist architectures; pattern collapse; LER smoothing methods; underlayer integration; new developers, etc.

Does this shift indicate that, in fact, EUV resists have become so successful as optical films that we are now free to mop up ‘minor’ engineering process details on the march toward manufacturing, or does it reflect something more fundamental?

This talk will delve into the materials science that underlies ultra-thin resist films (and ultra-small resist patterns) and attempt to assess how well findings in this field can account for the observed shift in EUV resist discussions. How are fundamental resist materials issues distinct from fundamental optical film issues? What experimental and simulation tools can be (and are being) used to understand phenomena such as interfacial perturbation of polymeric structures, mechanical properties of ultra-small polymer beams, and key pattern development effects such as interfacial swelling and gelation? Finally, what continuing R&D challenges are materials behaviors in the EUV size regime likely to pose as EUV lithography matures, and how distinct are they relative to challenges seen at longer wavelength lithographies?

IMPACT Center Research in Double Patterning: flavors, performance metrics, design restrictions

Kameshwar Poola
poolla@berkeley.edu

The IMPACT Center is a collaboration of researchers at UC Berkeley, UC San Diego, and UCLA, funded by 18 semiconductor companies and the State of California. Our research aims to closely integrate process, design, modeling and computation to develop technologies that will enable manufacture at the 20 nm node and beyond. I will offer an abbreviated survey of our recent results in double patterning. Following this, we will discuss key research questions that drive our research in double-patterning – defining appropriate performance metrics beyond minimal number of stitches, the role of design restrictions for making decomposable layouts, and layer-specific double patterning flavors. We conclude with a candid assessment of the impediments of conducting relevant research on double-patterning in academia – limited data access, avoiding wild goose chases, and untangling IP issues.

Can High Density 3D Through Silicon Stacking replace lithography-driven CMOS scaling as the engine for the semiconductor industry?

Matt Nowak
Senior Director, Advanced Technology
Qualcomm CDMA Technology Division

A view of the status, manufacturing readiness, and key challenges of high density 3D Through Silicon Stacking (TSS) will be presented. High density 3D TSS offers opportunities for cost reduction, performance and energy improvement, and form factor miniaturization for advanced semiconductor systems, with strong dependence on the system architecture and application. We will explore the cost reduction opportunities of HD 3D TSS compared to traditional System on Chip (SOC) solutions enabled by lithography-driven CMOS scaling. As the industry moves to EUV lithography at 16nm and below, the economic improvement resulting from CMOS scaling is expected to diminish. Architectural and software innovation enabled by HD 3D TSS and Architectural Pathfinding could provide an additional vector for continuing the improvements from semiconductor miniaturization.

Session 7

Presentation Schedule for
Wednesday, November 10, 2010

Time	Presenter	Title
8:00 – 8:50 AM	**John Warlaumont** ***Plenary Speaker***	**Turning seedlings into trees: The success of consortia (SEMATECH) in bridging technology and funding gaps**
8:50 – 9:15 AM	Andrezej Strojwas	Connector based designs to enable pattern controlled library for 22/20nm lithography
9:15 – 9:40 AM	Andreas Wild	An ecosystem approach to double patterning: the ENIAC JU project "LENS"
9:40 - 10:05 AM	Paul Nealey	Block copolymer lithography
10:05 – 10:35 AM	BREAK	

Turning seedlings into trees: The success of consortia (SEMATECH) in bridging technology and funding gaps

John Warlaumont
SEMATECH

The semiconductor industry has delivered a continuous, unparalleled stream of electronic chip technology innovations for more than 4 decades, and these innovations have been the primary driver of productivity growth for the world economy for that period. The need for this growth in technology capability continues unabated, with many industries (including communications, games, automotive, health care, and energy) requiring better technology to sustain their growth.

Today there are many programs around the globe focused on generating new technology ideas, but the challenges of turning these ideas into practical and available solutions have never been greater. These challenges are both technological and financial and are in many cases either pre-competitive or beyond the wherewithal of a single institution.

A growing set of innovative or strengthened collaborations is emerging to meet both the technology development and infrastructure viability requirements of technology growth. These collaborations are taking place in the USA (with a strong program in NY), in Europe, and in Japan. New programs are being established in lithography (EUV infrastructure and maybe multi-column e-beam infrastructure), 3-D interconnect (especially eco-system development), post-silicon devices for logic and memory, and magnetic storage. These programs are enabled by an unprecedented level of international collaboration and include significant partnering of chip makers, equipment makers, and materials suppliers. SEMATECH and NYS in Albany have been especially active in growing infrastructure viability.

Connector based designs to enable pattern controlled library for 22/20nm lithography

Tejas Jhaveri & **Andrzej J. Strojwas**
PDF Solutions, Pittsburgh, PA

Source mask optimization (SMO) has been demonstrated to be a valuable technology to enable low-k_1 single exposure lithography. The improvement in lithographic capability enabled by SMO has made it evident that it would be an integral part of most double patterning technology (DPT) flows. However, the single most crucial requirement for SMO is that layout patterns across the chip be consistent and constrained. PDF Solutions has developed a pattern constrained library that is demonstrated to be SMO compatible. In this methodology, the layout fabric constraints are provided to the designers in the form of base template and connector templates. Designers can then create cell libraries using an array of base templates and several instantiations of connector templates. The use of this methodology enables a 25X pattern count reduction compared to gridded logic layouts and is the only solution available that ensure pattern count saturation within a 100um x 100um random logic block. Results on SMO compatibility have been demonstrated in the collaborative work between ASML and PDF Solutions and published in a joint paper at Photomask Japan 2010. The work highlighted the benefits of developing layout fabric in conjunction with SMO to not only eliminate iterations between SMO and design but also to maximize process window (PW) for both SRAM and random logic. In one particular example, a 19.5% improvement PW was demonstrated by slight modifications of SRAM bit-cell layout. In this presentation we will discuss the development of the optimal fabric for SMO and DPT compatibility, the definition of the base template and corresponding connector templates to provide the fabric constraints and results highlighting the cost-effectiveness of this approach to 22/20nm and below.

An ecosystem approach to double patterning: the ENIAC JU project "LENS"

Andreas Wild
Andreas.Wild@eniac.europa.eu

The ENIAC Joint Undertaking, a European public-private partnership, provides grants to collaborative R&D efforts on strategic topics. The projects are proposed by consortia, judged by a panel of independent experts and selected for funding by public authorities. This approach federates key contributors in an eco-system, enticing them to innovate, assume leadership and advance the state of the art in their area of expertise and interest; the consortium as a whole is in the position to address in a synergetic way various aspects of a difficult challenge. The ENIAC JU project "LENS" is testing the applicability of double patterning techniques for the next nanometric generations. Following this bottom-up, self structuring paradigm, it brings together all elements of the supply chain to accelerate advances in design and mask generation, materials, exposure tools, metrology, and cost of ownership optimization, driving both the double exposure and the pitch doubling processes towards maturation, and then let the best win.

Block copolymer lithography

Paul Nealey
University of Wisconsin

The research program at the University of Wisconsin (UW) aims to integrate self-assembling block copolymers into the lithographic process. The fundamental concepts of the UW approach are that 1) the most advanced production-oriented exposure tools (e.g. 193 nm, EUV, or electron beam lithography) and resist materials are used to create patterns of differing chemical functionality on the substrate, and 2) films of block copolymers can be directed to assemble in the presence of the chemical pattern into predictable and desirable morphologies, thereby augmenting and enhancing the lithographic process. In comparing the pattern in resist to the pattern of domains induced to assemble in the block copolymer film, directed assembly has been demonstrated to achieve high degrees of pattern perfection, placement of features at the precision of the lithographic tool used to make the chemical pattern, improved dimensional control of features, improved line edge and line width roughness, and resolution enhancement by factors of two to four. In addition, the UW approach has been demonstrated to robustly achieve non-regular device-oriented geometries used in the fabrication of integrated circuits also with resolution enhancement by multiplication of feature density by interpolation on low duty cycle chemical patterns. After describing current capabilities, remaining technological questions and pathways towards implementation in specific applications will be discussed.

Session 8

Presentation Schedule for
Wednesday, November 10, 2010

Time	Presenter	Title
10:35 – 11:00 AM	SV Sreenivasan	Status of Jet and Flash Imprint Lithography Tool and Process Technology
11:00 – 11:25 AM	Bruno LaFontaine	Performance of a Laser Produced Plasma EUV source
11:25 – 11:50 AM	Yu Cao	New Applications of Computational Lithography Using Predictive Scanner Models
11:50 AM – 12:15 PM	Hank Smith	Maskless Photolithography for Customization
12:15 – 12:40 PM	Andrew Grenville	Imageable Oxides: New Solutions for Resist
12:40 PM	End Session	

Status of Jet and Flash Imprint Lithography Tool and Process Technology

S.V. Sreenivasan
UT-Austin and Molecular Imprints, Inc.
Nanoimprint Lithography Session
Lithography Workshop, November 7-11, 2010

Nanoimprint lithography techniques are known to possess remarkable replication capability down to sub-5nm resolution. Translating this nano-scale resolution to a commercially viable manufacturing approach requires development of tools, materials, masks and processes that can achieve reliable nano-scale performance at reasonable cost.

In recent years, a form of UV imprint lithography known as Jet and Flash Imprint Lithography (J-FIL) has seen significant progress in mask infrastructure, materials, CD control through etch, defect reduction, overlay, and throughput. This progress has opened up emerging nanomanufacturing applications for J-FIL such as patterned media for hard disk drives; and as a complement to photolithography at sub-25nm half-pitch nodes for semiconductor ICs.

The speaker will provide the current state of J-FIL technology in applications such as terabit density magnetic storage and advanced solid state memory. He will discuss both stepper tools as well as whole substrate patterning tools developed using the J-FIL technology.

Biographical Summary:

S.V. Sreenivasan is a Professor and the Thornton Centennial Fellow in Engineering at the University of Texas at Austin. He is also a Founder and Chief Technology Officer of Molecular Imprints, Inc. His research is in the area of high throughput nanomanufacturing as applied to high density memory, nano-electronics, photonic devices, and emerging biomedical and clean energy applications. S.V. has published over 100 technical articles and holds over 60 U.S. patents in the area of nanomanufacturing. He has received several awards for his work including Technology Pioneer Award by the World Economic Forum in 2005, The American Society of Mechanical Engineers Leonardo da Vinci Award in 2009, and the 2010 O'Donnell Award in Technology Innovation conferred by The Academy of Medicine, Engineering and Science of Texas (TAMEST).

Performance of a Laser Produced Plasma EUV source

Bruno La Fontaine
Cymer, Inc.

The first Laser Produced Plasma sources for 0.25 NA EUV scanners are being delivered to users this year. In this paper we report on the status of integration and testing of several sources destined for users and for internal learning. We also discuss the integrated performance of these sources in terms of power, dose stability, far-field EUV intensity distribution, as well as the performance of sub-systems such as the drive laser, tin droplet generator and collector. Finally, we review the remaining challenges associated with higher power operation, which will enable the scanner throughput required for high volume manufacturing, and the plans being put in place to support this level of performance.

New Applications of Computational Lithography Using Predictive Scanner Models

Yu Cao
Brion/ASML

Predictive scanner models make use of optics design information and describe how the optics behaves in response to setting changes or manufacturing effects. These models, when integrated with lithography simulation, allow the exploration of scanner optics and imaging effects in a cost-effective and systematic manner. In addition, new manipulators such as FlexRay and FlexWave on ASML scanners provide many new degrees of freedom and opportunities for optimization. In this paper, we describe predictive models for the illumination and projection optics for ASML scanners, and their applications to proximity matching, hotspot reduction, process window enlargement, and lens heating control.

Maskless Photolithography for Customization

Henry I. Smith, M. Walsh, F. Zhang, J. Ferrera, G. Hourihan, M. Jaspan
LumArray, Inc.
15 Ward St.
Somerville, MA 02143
www.lumarray.com

Lumarray has developed a maskless-photolithography system, the ZP-150, based on zone-plate-array lithography (ZPAL). It employs an array of 1000 diffractive-optical lenses to focus light from a spatial-light modulator (SLM) into on-axis focal spots. By scanning the stage across the entire substrate, while controlling the light level to each focal spot, patterns of arbitrary geometry are written in a dot-matrix fashion. In contrast to other maskless-lithography approaches, the ZPAL architecture lends itself to straightforward enhancements in thruput, resolution, precision, overlay, 3D structuring and non-planar substrates. For thruput enhancement, the number of lenses or the SLM data rate can be increased. For resolution enhancement, the wavelength can be reduced or methods such as AMOL employed. Precision and overlay can be enhanced via software. 3D structuring and non-planar surfaces can be addressed with special diffractive-optical lenses. The design choices, current performance, future plans and the application space for Lumarray's systems will be described.

Imageable Oxides: New Solutions for Resist

Andrew Grenville
Inpria

Inpria is developing a directly patternable, inorganic hardmask platform for lithography. The approach is based on photosensitive metal oxide sulfate films deposited from aqueous solutions. The films are atomically smooth, dense, and amorphous, providing the basis for high-fidelity patterning. The material is capable of achieving a resolution of 10 nm half-pitch, and LWR of 1.6 nm at 30 nm half-pitch via electron-beam lithography. We have also tuned it for exposure by EUV or 193nm. The high absorbance of the films and the efficient exposure chemistry provide a path to commercially relevant sensitivity. In addition, because the exposure process does not rely on chemical amplification, especially low resist blur is observed. Ultra-thin (20 nm) imaging layers can be employed since film integrity is readily retained at these thicknesses and the material itself performs as a very highly selective etch mask. This mitigates pattern collapse and can reduce pattern transfer steps.

Session 9

Presentation Schedule for
Thursday, November 11, 2010

Time	Presenter	Title
8:00 – 8:25 AM	Michael Thompson	Sub-millisecond Post-Exposure and Hard Bake of Chemically Amplified Photoresists.
8:25 – 8:50 AM	Joy Cheng	Directed Self-Assembly for Lithography Applications
8:50 – 9:15 AM	Franklin Kalk	Advanced photomasks: challenges and choices
9:15 – 9:40 AM	Rudi Hendel	Extending the Limits - Embracing Restrictions:a scenario of future patterning technology.
9:40 - 10:05 AM	Andrew Neureuther	Physics-Based Models for Process Awareness
10:05 – 10:35 AM	BREAK	

Sub-millisecond Post-Exposure and Hard Bake of Chemically Amplified Photoresists

Byungki Jung, Christopher K. Ober and **Michael O. Thompson**
Department of Materials Science and Engineering, Cornell University, Ithaca NY 14853

Todd R. Younkin and Manish Chandhok
Intel Corporation, Hillsboro, OR 97124

Chemically amplified resists (CARs) continue to be developed to achieve sub-22 nm lithography in both 193i and EUVL platforms, with key challenges still in resolution, sensitivity and line width roughness (LWR). In this work, we explore the use of laser thermal processing to address these challenges by shifting the time/temperature regime for the post-exposure bake (PEB) process from 10's of seconds at 90-130^{o}C to sub-millisecond times at temperatures of 250-450^{o}C. For resists with a high activation energy for deprotection compared to acid diffusion, the shift to high temperatures should enhance the sensitivity with no loss of resolution, and potentially improve LWR from the polymer flow at high temperature.

Sub-millisecond laser PEB (*l*-PEB) is achieved using a CW CO_2 laser source focused to a narrow line and scanned across the wafer. The effective time at temperature is controlled by the beam width and the scan velocity to times ranging from 200 μs to 5 ms, with peak temperature set by the laser power. Nine resist/PAG systems were studied to establish resist sensitivity and acid diffusion under *l*-PEB. Imaging under EUVL showed a nearly three times enhancement in resist sensitivity over hot-plate PEB (for comparable resolution) with an ~20% reduction in LWR.

To understand this behavior, kinetic rates of deprotection and acid diffusion were quantitatively determined as a function of hot plate and *l*-PEB temperature and duration. While diffusion in the two regimes follow a common activated behavior, the deprotection rates differ by nearly three orders of magnitude between seconds scale and millisecond scale heating (Figure 1). Results suggest a strong coupling between the temperature ramp rate during PEB and deprotection behavior of CARs. Possible mechanisms, and experimental tests, to explain this behavior will be discussed.

In a second approach to LWR control, we have examined use of the scanned laser source to anneal fully developed resist patterns at peak temperatures of 200-400^{o}C – a sub-millisecond laser hard-bake. We hypothesize that patterned resists above their glass transition temperature will flow to minimize the surface energy resulting in reduced line edge roughness. Figure 2 shows SEM images of 30 nm half-pitch lines before and after laser annealing at 22W (~200^{o}C) for 500 μs. Dramatic smoothing (reduced LWR) of the lines is immediately evident and likely a direct consequence of resist flow at temperatures above T_g. Characterization of LWR reduction for different CARs and models to explain the behavior will be presented.

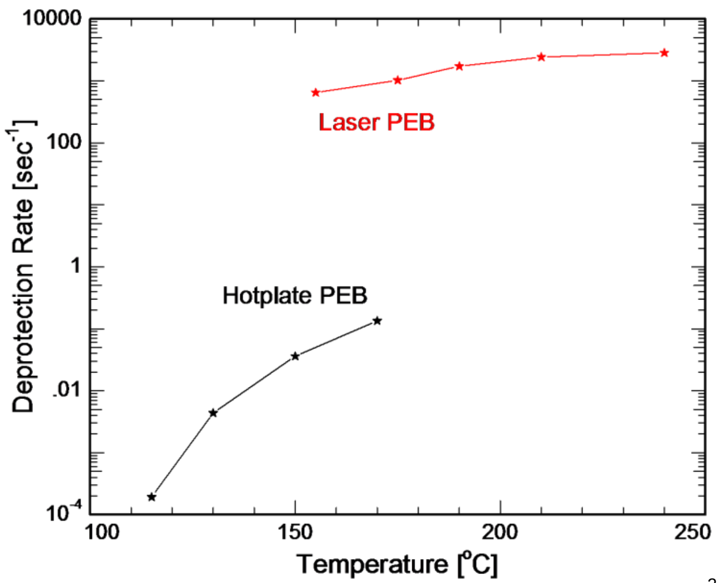
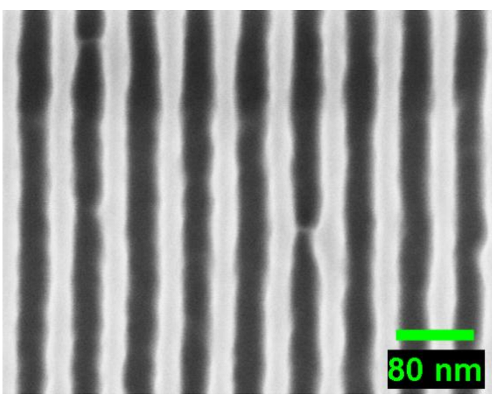


Fig. 1. Deprotection rate as a function of temperature at a fixed E_0 = 3 mJ/cm^2. Data exhibit 10^3-10^4 enhancement in deprotection between hot plate PEB and *l*-PEB.

a) 

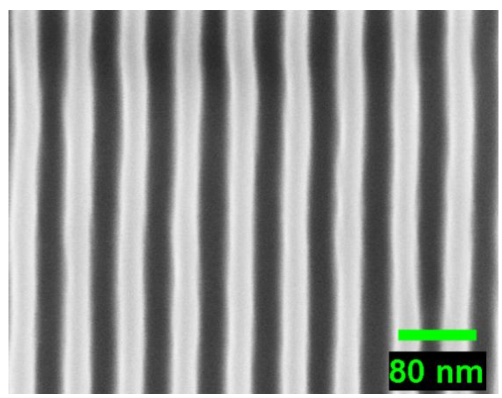
b) 

Fig. 2. SEM images of 30 nm line/spacing under a) conventional EUVL and b) conventional EUVL followed by laser heating at 22W (~200^{o}C) for 500 μs.

Directed Self-Assembly for Lithography Applications

Joy Cheng
IBM Almaden Research Center

Directed self-assembly (DSA), which combines self-assembled polymers and substrates with lithographically-defined directing prepatterns, has been considered as a potential candidate to extend the resolution limit of conventional lithography. Frequency multiplication and pattern rectification have been successfully demonstrated using block copolymers on patterned substrates defined by various lithography techniques. Collaborating with research partners, we hope to address important issues, such as track compatibility and DSA performance, in the integration of DSA into standard lithography. We developed track-compatible DSA process and materials which provide a simple and straight forward DSA platform to generate sub-lithographic line-space patterns and vias. Critical parameters for DSA performance such as DSA materials, directing prepatterns, and their interactions are systematically investigated using experiments and simulations.

Advanced photomasks: challenges and choices

Franklin Kalk

Along with the rest of the semiconductor lithography infrastructure, mask manufacturing is experiencing a sea-change at the leading edge. Double patterning, EUV, direct write, and nanoimprint are all contenders to extend the industry's scaling success to 2020. Are we faced with an embarrassment of riches or a closet full of skeletons?

This paper employs several criteria to examine the candidate technologies: technical challenges, specifications, extensibility, cost, and application space.

"Extending the Limits - Embracing Simplicity"
A scenario of a future patterning technology:
Accepting Periodicity for Cost Effective Patterning and Ultimate Resolution

Rudi H. Hendel; Periodic Structures Inc. (Presenter)
John S. Petersen; Periodic Structures Inc.
David A. Markle; Periodic Structures Inc.
Robert Greenway; Periodic Structures Inc.
Mike Smayling; Tela Innovations Inc.

Semiconductor Manufacturing faces significant challenges on reaching the dimensions required in future generations of Integrated Circuits. No satisfactory manufacturing solutions exist for a pitch of <50nm while EUVL, Optical Lithography Extensions, Sidewall Patterning, e-beam based Multi-beam Maskless and Imprint Technologies vying for selection.

Restricting patterns to high regularity removes a long list of increasingly complex Design Rules and promises a number of benefits for a cost effective solution. To become a reality, this will require future designs to have layout restrictions tied to high regularity built into their libraries.

We will present the benefits that we expect from Interference Assisted Lithography, discuss key challenges to be met before the technology can be inserted into manufacturing and consider the trade-offs to be made in simplifying the layouts to patterns consistent with Interference Technology.

Physics-Based Models for Process Awareness

Andrew R. Neureuther[1], Juliet Rubinstein[1], Eric Chin[1], Lynn Wang[1], Marshal Miller[1], Chris Clifford[1], and Kenji Yamazoe[2, 1]

[1]*231 Cory Hall, Department of Electrical Engineering and Computer Science, University of California Berkeley, California, 94720-1770, USA*

[2]On leave from *Canon Inc., 23-10, Kiyohara-Kogyo-danchi, Utsunomiya-shi, Tochigi-ken, 321-3298, JAPAN*

Corresponding author: neureuth@eecs.Berkeley.edu

Results will be reported on a variety of projects that enable moving physical understanding upstream in the circuit design process with fast-CAD approaches. Measured parameter-specific ring-oscillator results for at 45 nm process in collaboration with the Berkeley Wireless Research Center and ST Micro show that individual devices vary by nearly 10%, only about 1/6 of this variation is due to LWR, and that on a good wafer the chip-to-chip variation for a 2 mm by 2 mm chip has an R^2 correlation of about 0.95 even among different RO circuit layouts suggesting that the correlation length is more than 1 mm. In pursuing fast through focus models, a new results is that the image in the presence of mild aberrations and mask phase effects of any pattern at three focal positions can be used to predict the image of that pattern to an accuracy of 1% at all defocus levels through + and – RU window from the same 4 coefficients calibrated from a contact hole pattern. The accuracy of kernel convolution pattern matching has been dramatically increased to an R2 level of 0.98 with rigorous simulation and still retaining a speed-up of 10^5 through utilizing separate matching at a small number of source sub-regions (Abbe style). The kernels for this method including aberrations and extra kernels for EM mask edge effects that tilt the process window can be generated automatically from any simulation program that computes the pupil function by subtracting the pupil function at two focus settings. EUV blank defects are harder to characterize and compensate in mask repair than DUV defects due to their phase, large lateral size from smoothing and the lateral propagation of EM effects in the multilayer substrate. At first look double patterning cuts of line arrays looks promising with electron-beams, but when the current decreases at a high power of spot size knowing that 45 instead of 10,000 electrons will suffice will make a big difference.

Session 10

Presentation Schedule for Thursday, November 11, 2010

Time	Presenter	Title
10:35 – 11:00 AM	Chris Bencher	An Assessment of Patterning Options for 15nm Half-Pitch
11:00 – 11:25 AM	Kevin Lucas	Pattern Splitting interactions with design density and OPC complexity
11:25 – 11:50 AM	Andrew Kahng	A Roadmap for DFM
11:50 AM – 12:15 PM	Chenson Chen	A Decade of SOI-Based 3DIC's at MIT Lincoln Laboratory
12:15 PM	End Session	

An Assessment of Patterning Options for 15nm Half-Pitch

Chris Bencher
Technical Staff, Applied Materials

Despite the challenges in scaling below 20nm half-pitch, several NAND-Flash manufacturers are pursuing 15nm technology nodes within the near future. Assuming the manufacturing leaders maintain their 2-year technology cycle, the need for 15nm half-pitch at pilot production volumes could be as soon as 2014; earlier than a 3rd or 4th generation EUV scanner could make 15nm single patterning an option. So, what are the alternatives?

By using various density multiplication techniques, 15nm half-pitch can be obtained by several techniques, each at different stages of maturity.

1. Spacer quadruple pattering on 120nm pitch lithographic pre-pattern (ArF dry).
2. Spacer triple patterning on 90nm pitch lithographic pre-pattern (ArF immersion).
3. Spacer double patterning on 60nm pitch lithographic pre-pattern (EUV)
4. Directed Self-assembly on lithographic pre-patterns of a relaxed pitch.

Applied Materials is collaborating with leading research groups to conduct 300mm wafer level assessments for these options. Spacer-quad patterning is currently the most mature, already showing performance near ITRS requirements; however, it comes with layout restrictions. Spacer-triple patterning is interesting because it allows multiple line-widths which give designers added degree of freedom over spacer double and quadruple patterning. Spacer-double pattering over EUV can leverage all the design rules, design tools, and process integration schemes created for the current generation of SADP devices. Directed Self-Assembly offers chemical based solutions to the current optical and diffraction based problems facing scaling.

In this presentation, we will discuss the merits and limitations of these various schemes, review wafer level data, and field questions related to the process maturity and experimental difficulties.

Pattern Splitting interactions with design density and OPC complexity

Kevin Lucas

A considerable number of device technology nodes and layers are currently considering or already using pitch splitting lithographic techniques to extend resolution below the physical K1=0.25 limit of traditional single exposure technology. In this talk we study the use of leading pitch splitting methods for the varied layouts found in random logic, SRAM or DRAM applications on different patterning levels. For both litho-process-litho-etch and self-aligned pitch splitting methods, we investigate design and OPC/RET/litho process interactions with RAM and random logic poly, local metal layers and routed metal layers including common non-compliant design occurrences and potential design restrictions.

A Roadmap for DFM

Andrew B. Kahng
UC San Diego

A technology roadmap consists of (1) measurable requirements, driven by (2) anticipated deployment contexts, with associated (3) potential solutions, at (4) specific points in time. Roadmapping of DFM is quite challenging, in that DFM seems needed mostly when all other competencies {SPICE modeling, design rule manual, circuit and layout design, design analysis and signoff, yield learning, process control, process equipment, …} fail. The ITRS roadmap for DFM mostly provides high-level linkages between process variations and parametric yields. At the same time, DFM in the late-CMOS era will require holistic understanding across litho option costs, design rule interactions, library and layout methodologies – even chip architectures. This talk will describe a possible set of technology metrics and a timeline for new technologies (i.e., solutions), within the context of an overall roadmap for DFM.

A Decade of SOI-Based 3DIC's at MIT Lincoln Laboratory

Chenson Chen
MIT Lincoln Labs

We have established a three-dimensional integrated-circuit (3DIC) technology based on fully depleted SOI (FDSOI) CMOS wafer tiers that are oxide-oxide bonded and interconnected by 3D tungsten plug vias. Our 3DIC technology has been developed and demonstrated over ten design cycles, bonding two or three active circuit layers or tiers to form monolithically integrated 3D circuits. An overview of our 3D process technology, including device characteristics and circuit results, demonstrating both mixed technology and mixed material 3D integration, will be presented.

Session 11

Presentation Schedule for
Thursday, November 11, 2010

Time	Presenter	Title
1:40 – 2:05 PM	James Blatchford	Streamlined simulation flows for assessing design rule and patterning choices for advanced logic nodes
2:05 – 2:30 PM	Juan de Pablo	A Molecular View of Block Copolymer Directed Assembly and its Application to Sub-Lithographic Patterning
2:30 – 2:55 PM	Carlos Fonseca	Employing cost-effective solutions in double patterning schemes
2:55 – 3:25 PM	BREAK	

Streamlined simulation flows for assessing design rule and patterning choices for advanced logic nodes

James W. Blatchford
Advanced CMOS Technology Development, Texas Instruments, Inc., Dallas, TX 75082

As device scaling progresses beyond the 28nm logic node, the economic challenges associated with lithography become almost as formidable as the technical challenges. In particular, in light of the uncertainty in cost and availability of EUV technology, many device manufacturers are now investigating double-patterning (DPT) and multi-patterning (MPT) strategies to achieve the required die area scaling with existing optical technology. The mask count for such approaches can be quite high, and the cost of multiple patterning must therefore be carefully justified by the amount of area shrink achievable, with cost-per-good-die becoming a critical metric for assessing design rule and patterning choices. Furthermore, the use of DPT/MPT in random logic introduces many additional rule restrictions that can greatly impact die area, complicating the analysis. To that end, we have developed a sophisticated infrastructure for (i.) streamlining design rule definition for 20nm and 14nm logic nodes assuming a number of single-exposure, double- and multiple-patterning techniques; (ii.) relating those rules to area scaling using a 'perturbative' place-and-route method with appropriately scaled standard cells; and, (iii.) combining these results with rigorous cost modeling to assess cost-per-good-die. In this paper, we discuss details of the simulation flow, and apply the infrastructure to assess patterning and rule choices for 20nm and 14nm logic nodes from the perspective of complexity and cost-per-die added. We further analyze implications of various strategies for restricting layout rules to enforce DPT/MPT compliance.

A Molecular View of Block Copolymer Directed Assembly and its Application to Sub-Lithographic Patterning

Juan J. de Pablo
Department of Chemical and Biological Engineering
University of Wisconsin - Madison
1415 Engineering Drive, Madison, WI 53706

Directed copolymer assembly (DCA) has emerged as a promising alternative for patterning at sub-lithographic length scales. Much progress has been made over the past decade, but a number of significant issues must still be addressed for DCA to find widespread use in commercial, large-scale processes. Recent demonstrations of DCA have shown that a number of variables can be used to control and optimize the directed assembly of copolymers on patterned substrates. These include the molecular weight of the polymeric constituents, the composition of the copolymers and their blends with homopolymers, the interactions between different blocks and different regions of a patterned the substrate, and the commensurability (or lack thereof) between a substrate pattern and molecular dimensions. Recent work has also shown that the morphologies that arise in DCA are often very different from those adopted by the same material in the bulk, reinforcing the fact that the copolymer thin film and substrate, together, must be regarded as a completely new system whose behavior is difficult to anticipate by simple extrapolation of bulk results.

Over the past decade, our group at the University of Wisconsin has adopted a truly concerted experimental and computational approach aimed at gaining a fundamental understanding of DCA on nanopatterned substrates. One aim of our efforts has been to identify suitable materials and determine optimal conditions for sub-lithographic patterning by DCA. Another aim of our work has been to interpret experimental data from micro length scales down to the level of individual patterns and molecules. This presentation will provide an overview of current theoretical and computational approaches developed in our group to arrive at that understanding[1,2], along with an in-depth analysis of advantages and limitations of existing DCA strategies. As will be shown in this talk, these approaches are truly predictive and rely only on knowledge of composition and molecular architecture of all components. They serve to predict different morphologies, the boundaries between them and, when imperfect states arise, they help determine the origin of defects.

Particular emphasis will be placed on issues pertaining to process latitude and robustness in the context of pattern interpolation and sub-lithographic patterning[3,4]. The overall goal is to rely on the spontaneous but controlled assembly of copolymers to arrive at dense patterns with characteristic dimensions in the tens of nanometers, while using sparse patterns defined on larger length scales. This presentation will discuss the issues that arise with DCA in the context of motifs of interest to the semiconductor industry. A comparison of results for various approaches, including chemical patterning and topographic patterning will also be presented. General correlations and design rules in terms of predicted free energy minima will be discussed for analysis of a number of experimental observations, including some related to pattern quality and process latitude.

---

1 F.A. Detcheverry et al., Soft Matter, 5, 4858-4865 (2009).
2 F.A. Detcheverry et al., Physical Review Letters, 102, Article Number 197801 (2009).
3 R. Ruiz et al. Science, 321, 936-939 (2008).
4 F.A. Detcheverry et al., Macromolecules, in press (2010).

Employing cost-effective solutions in double patterning schemes

Carlos Fonseca
carlos.fonseca@us.tel.com

Double patterning (DP) techniques have generally gained acceptance by many IC makers as a solution to continue device scaling at 193nm wavelength. Given that EUV lithography (single exposure) is still maturing, several DP implementations have gained traction in specific applications (lithographic layers). In general DP techniques enable higher density and feature scaling with added complexity and cost implications – A trade-off that must be well-balanced for cost effective solutions.

In this work we present and discuss how the wafer track has evolved over time to support and meet performance and cost effectiveness in DP schemes. In addition, we discuss potential DP schemes/strategies and their impact to implementation and cost benefits.

Session 12

Presentation Schedule for Thursday, November 11, 2010

Time	Presenter	Title
3:25 – 3:50 PM	Rick Uchida	Advanced PAG design for chemically amplified resists
3:50 – 4:15 PM	John Warlaumont	Accelerating the introduction of 3D TSVs at SEMATECH
4:15 – 4:40 PM	Ed Holland	Roll to roll imprint lithography for flexible electronics and structural templates.
5:00 PM	End Session and Conference	

Advanced PAG design for chemically amplified resists

Rick Uchida

In optical lithography, chemically amplified resist (CAR) is a common chemistry platform used in a variety of applications to obtain resolution as far as sub 30nm half-pitch targets. The pattern quality control through photo acid generator (PAG) optimization in CAR is one of the key challenges as the semiconductor industry continues to increase the number of transistors in accordance to Moore's law. PAGs of different characteristics, such as acid strength and diffusion length, were synthesized to study the resist performance improvement. In these PAG molecular design study, we observed that acid diffusion coefficient (D) was not only influenced by the anion molecular size, but the molecular interaction between the exposure induced acid and polymer matrix as one of the key factor in determining D.

Accelerating the introduction of 3D TSVs at SEMATECH

John Warlaumont
VP, Advanced Technology
SEMATECH

Through Silicon Via technology has been studied for the last two decades, and is now being considered the interconnect technology of choice for performance, scaling, power and density improvements. However, gaps in technology and infrastructure readiness remain, and this talk covers the efforts at SEMATECH to address both areas in order to ease the introduction of 3D TSVs into high volume manufacturing.

Roll to Roll Imprint Lithography for Flexible Electronics and Structural Templates

Ed Holland
HP Labs
Nanoimprint Lithography Session
Lithography Workshop, November 7-11, 2010

Imprint lithography techniques developed at HP have demonstrated a diverse range of capabilities. Compatibility with a wide range of materials, multiple use modes and the potential for large scale production represent the strengths of this technology. In this paper, two examples of development are presented to illustrate the potential for application of imprint lithography to quite different tasks. In the first case, imprint lithography is a facile component in the development of roll-to-roll processing methods for flexible electronic circuits. The technique of Self Aligned Imprint Lithography (SAIL) is presented in overview. In this approach, micron scale mask patterns, comprising multiple levels for all required patterning steps are formed by one imprint action on a continuous web of material. Processing of a predeposited stack of electronic materials is thus enabled without the repeated alignment procedures required in conventional multi-step lithography. This offers a dual advantage, allowing the processing of dimensionally unstable materials and enabling the use of continuous roll-to-roll process methods. The fabrication of flexible thin film transistor (TFT) arrays for electrophoretic displays will be presented as a process example. In a second aspect of HP's work, the application of imprint lithography to create functional structures will be introduced. We have explored the capability of imprint processing to generate high aspect ratio structures e.g. for fluid containment. Arrays of transparent well structures, formed on a flexible transparent substrate provide the basis for a color filter matrix that is filled by inkjet deposition of pigmented resins. The advantages of this approach in terms of precise color pattern definition will be presented. Components patterned with high absolute precision by imprint lithography were readily integrated with parts from other sources to yield flexible color reflective display demonstrator panels.

Poster Papers

Monday, November 8, 5:00 – 7:00 PM
Tuesday, November 9, 5:00 – 7:00 PM

Presenter	Title
Eric Chin	Variability Aware Standard Cell Timing Libraries
Dan Soltman	Modeling inkjet printing
Stewart Robertson	Stochastic Simulation of Resist Effects on Roughness and Uniformity at EUV
Jim Jacob	Long coherence length sub-200 nm light source for full-field interference lithography
Rajesh Menon (presented by Hank Smith)	Novel Photochemistry enables Deep sub-wavelength Optical Nanolithography
Hiroshi Morita	Molecular level simulation of the development and the rinse processes
Hidetami Yaegashi	The self-aligned spacer Double Patterning process toward 11nm node and beyond

Variability Aware Standard Cell Timing Libraries

Eric Chin
UC Berkeley

Standard cell timing variations are caused by process non-idealities that are not traditionally captured by standard cell timing characterization tools. Our research presents an alternative approach by characterizing standard cells in the presence of process variations to develop compact variability aware timing models that can be incorporated into existing standard cell timing libraries. This enables static timing analysis tools to perform critical path variability aware delay analysis using a presumed layout-dependent distribution of process parameters.

To develop these variability models, we utilize a novel methodology that combines rigorous process simulation, contour-based non-rectangular transistor analysis, and timing characterization. Multiple layout contexts are generated. Then optical proximity correction (OPC) and lithography simulation are performed across a focus exposure process window . At each process condition, the contour of each transistor is extracted to generate an equivalent device model for circuit simulation. Circuit simulation is then performed using equivalent device models to obtain the overall delay response. Finally, the delays are aggregated to fit a gate level compact delay model.

Using this characterization methodology, the delay responses for two standard cells in the Nangate 45nm Open Cell Library are shown to exhibit Bossung like behavior, and are visualized in an electrical process window. This technique is applied to standard cells to investigate focus exposure variations, corner rounding, and layout proximity effects. Variability aware timing models for standard cells in the form of delay variability tables or compact parameter timing models are shown to enable static timing analysis tools to perform variability aware delay analysis on critical paths with little expense in runtime.

Modeling inkjet printing

Dan Soltman

Inkjet printing is widely used as a maskless lithography technique for the fabrication of printed electronic devices. Here we present an analytic treatment of the inkjet printing of two dimensional patterns with a partially wetting ink. We develop and experimentally demonstrate an algorithm for generating the variable line spacings that lead to printed features superior to those possible with a standard, fixed-spacing raster-scan pattern. However, we find that tracking jetted volume alone is insufficient to optimize printed films since evaporative solvent loss during printing at any size scale proves to be significant. By exploiting radial symmetry, we are able to indirectly measure evaporation as jetting proceeds. Through accurate droplet shape modeling and volume tracking we are able to hold a growing bead's contact angle at its optimum value as it is printed, leading to, for example, squarest squares. An examination of the analytic solution for a rectangular bead's surface reveals a contact angle that falls to zero as the contact line approaches a corner. Substituting a growing circular arc into a sharp corner monotonically increases the corner contact angle. Thus, we are able to define the achievable corner fidelity for a given set of advancing and retreating contact angles, properties of a given ink-substrate system.

Stochastic Simulation of Resist Effects on Roughness and Uniformity at EUV

John J. Biafore, Mark D. Smith, **Stewart A. Robertson**, Trey Graves

KLA-Tencor, FINLE Division
8843 N. Capital of Texas Highway
Austin, TX 78759

Accurate and flexible simulation methods may be used to help a researcher's understanding of how complex resist effects influence the patterning of nanoscale structures. Historically, modeling strategies for optical lithography have applied the continuum approximation to the physics being simulated. However, the real world is discrete: light energy is made up of photons; chemical concentration has no meaning at a point, etc. Stochastic resist simulation allows prediction of responses that naturally arise from random fluctuations in lithography, such as LWR and CD uniformity. In this work, we attempt to gain insight into the behavior of several resist effects upon roughness and uniformity using stochastic resist simulation at EUV. The parameters of a well-calibrated EUV stochastic resist model are used as the initial condition. The parameters are logically varied and the effects of properties such as the exposure dose, exposed quantum yield, acid generator loading, kinetics of reaction-diffusion-development upon feature roughness and CD uniformity are discussed.

Keywords: EUV, stochastic simulation, LWR, CD uniformity

Long coherence length sub-200 nm light source for full-field interference lithography

Jim Jacob, Actinix
Darrell Armstrong, Sandia National Labs
Arlee Smith, AS Photonics
John Burnett, NIST
Eric Benck, NIST

Interference lithography has long been used as a simple maskless method to expose wafers with fine-pitched gratings over small field sizes (approximately 1 mm) in order to test photoresists in advance of full-blown lithographic scanners becoming available at each semiconductor process generation. Recently there has been interest in using liquid immersion interference lithography to enable the low-cost nano-fabrication of advanced application specific integrated circuits that are produced in low volumes. In this hybrid lithography scenario a grating with a half-pitch of approximately 35 nm is exposed over a full field (26 by 33 mm) as a first critical layer that is subsequently trimmed and stitched with a complementary technology (such as an e-beam or optical tool) to provide circuit functionality. The interference exposure tool requires a long coherence length laser source with a spatially pure transverse mode in order to print uniform gratings with both high contrast and high resolution. The large field size dictates a higher power and a longer coherence length than was previously used on the small field interference test tools. We will describe the development of a quasi-CW 197-nm laser system with preliminary design goals of over 250 milliwatts of average power and a coherence length of approximately ¼ meter (0.05 pm bandwidth). This solid-state laser source is expected to be capable of exposing up to ten wafers per hour assuming a photoresist dose requirement 50 mJ/sq-cm. We will also describe the metrology being designed to provide feedback to the laser source and to the optical exposure apparatus to control the pitch, field curvature and registration of the printed grating pattern.

Novel Photochemistry enables Deep sub-wavelength Optical Nanolithography

Nicole Brimhall, Trisha L. Andrews[1], Rajakumar Manthena and **Rajesh Menon***
Department of Electrical and Computer Engineering, University of Utah, Salt Lake City, Utah 84112
[1]Department of Chemistry, Massachusetts Institute of Technology, Cambridge, MA 02139
**rmenon@eng.utah.edu*

Nanostructures and devices have found applications in fields as diverse as health sciences, molecular electronics and renewable energy. Controlled manufacture of nanostructures became possible with the advent of scanning-electron beam lithography (SEBL). However, SEBL is a slow, serial process and hence, unsuitable for patterning nanostructures over useful areas. Optical lithography, on the other hand, enables parallelism while avoiding complexity brought about by high-vacuum and high-voltage requirements. However, conventional optical lithography is limited by diffraction to feature sizes greater than about half the wavelength.

In the past, we developed absorbance modulation to overcome this limit.1 This approach utilizes

photochromic molecules that can be optically switched between two thermally stable states, one opaque and the other transparent. When a layer of this material is exposed to a focused bright spot at λ1 (the wavelength that converts from the opaque to the transparent form) and simultaneously to a focused node at λ2 (the wavelength that reverses the transformation), the ensuing photochemical equilibrium results in a sub-wavelength transparent region in the vicinity of the node. Photons at λ1 penetrate this region forming an optical nanoscale probe. The lateral size of this probe is not limited by diffraction, but by material parameters and the ratio of the intensities at the two wavelengths. *In other words, optical near-fields are generated from afar*.

Absorbance modulation is limited to surface (2-D) patterning. Here, we also report on an alternative approach that exploits unique combinations of spectrally-selective reversible and irreversible photochemical transitions to achieve deep subwavelength resolution with potential extension to 3 dimensions. This approach, which we refer to as Patterning via Optical-Saturable Transformations (POST) has the potential for massive parallelism, enabling the creation of nanostructures and devices at a speed far surpassing what is possible with SEBL. In this presentation, we will describe our progress in the development of absorbance modulation for multiple exposures (to create dense patterns) and also present preliminary results from POST.

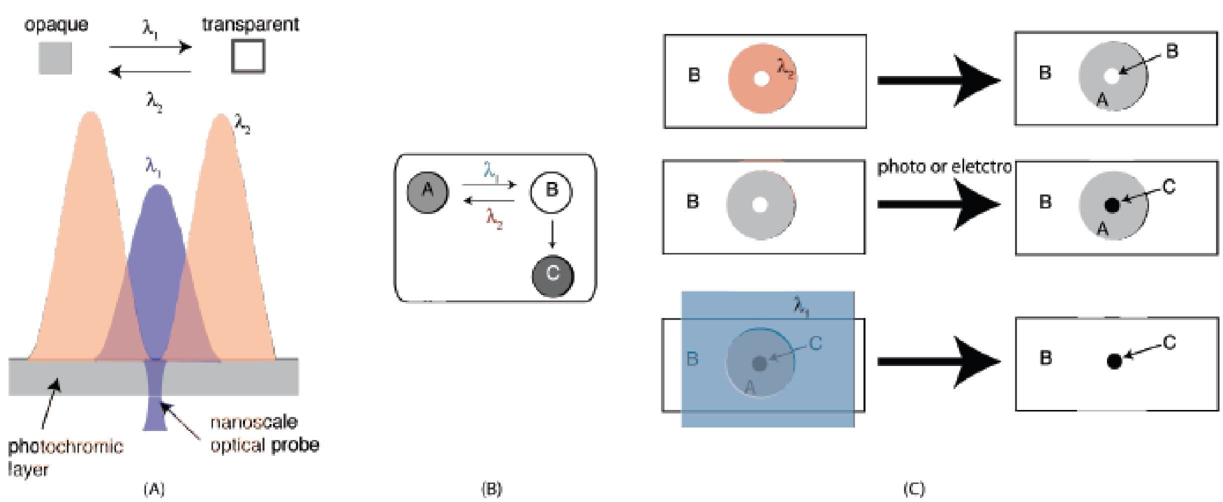


Fig. 1: (A) Scheme of absorbance modulation. (B) Molecular transformations required for POST. (C) Sequence of steps to create a deepsubwavelength region in a form C that is distinct from neighbors. The isomer-selective irreversible transformation from B to C may be electrochemical as indicated in Fig. 2 or photo-initiated.

1 T. L. Andrew, H-Y. Tsai and R. Menon, "Confining light to deep sub-wavelength dimensions to enable optical nanopatterning," *Science*, 324,
217 (2009).

Molecular level simulation of the development and the rinse processes

Hiroshi Morita (AIST), Ichiro Okabe, Saurabh Agarwal, Vivek Singh (Intel)

We analyze the dynamics of photoresist polymer chains during development and rinse processes, using a meso-scale simulation technique called Dissipative Particle Dynamics (DPD), where several neighboring monomers in a polymer chain are represented by one DPD particle to accelerate polymer dynamics simulation. In the development step, the simulation cell consists of DPD resist polymer particles in the lower part, and developer molecules in the upper part. For a positive tone resist, the exposed DPD particles dissolve in the developer, rendering the unexposed ones insoluble. After development, the rinse process is simulated and line edge roughness (LER) is evaluated.

In this presentation, we first provide an overview of the model and then demonstrate our simulation results such as the dynamics of the resist polymer development, and line edge roughness (LER) after the rinse process.

The self-aligned spacer Double Patterning process toward 11nm node and beyond

Hidetami Yaegashi
Tokyo Electron LTD, 650 Mitsuzawa, Hosaka-machi, Nirasaki City,Yamanashi, Japan

Introduction

Double Pattering process is one of the most promising lithography techniques for sub-40nm half-pitch technology node. Especially, Self-aligned spacer Double Patterning (SADP) has been adopted in NAND Flash memory devise manufacturing for 3X nm technology node and beyond. The uniqueness of our proposed SADP scheme is the utilizing of ultra-low temperature SiO_2 film deposition for spacer pattern with photo-resist core pattern. It would contribute to simplify the process steps and to minimize any process deviations.

In this study, we would mention further more optimization of Pitch-Quadrupling using SADP and 2D pattern fabrication for 2X nm technology node and beyond.

Results & Discussion

Successful demonstration of Pitch-Quadrupling for 11nm node pattern fabrication was produced. And the random 2D pattern utilizing SADP was feasible to describe. In this paper, it can be proven that Double Patterning process can extend the current 193-nm immersion technique to 22nm node and beyond.

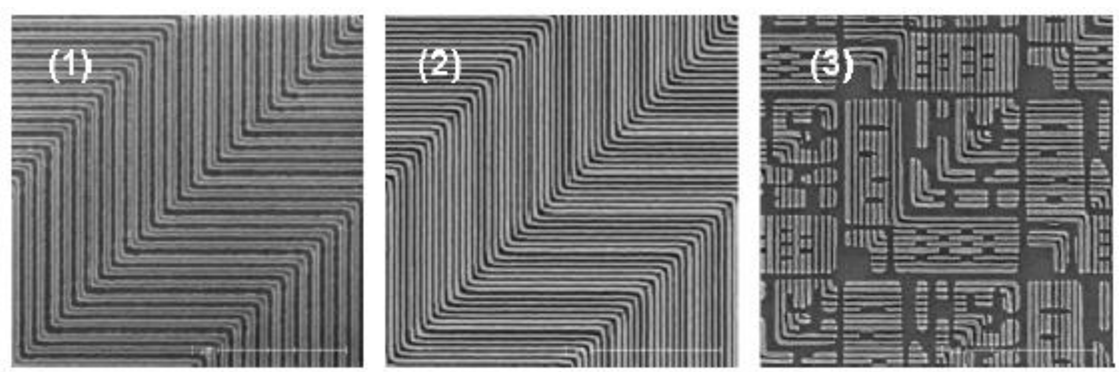


Fig-1 Demonstration result of complex 2D pattern through SADP

(1) 40-nm resist pattern,

(2)20-nm PolySi pattern after pitch doubling,

(3) 20-nm 2D pattern after cutting litho. Step

The Lithography Workshop gratefully acknowledges the Support of our Sponsors

Gold Sponsor

Luminescent TECHNOLOGIES™

Bronze Sponsors

ASML tok Ultratech

General Sponsors

Agilent Technologies

APPLIED MATERIALS®

Benchmark TECHNOLOGIES

CYMER

DARPA

DNP The Dai Nippon Printing Group

intel

JEOL

KLA Tencor

Mentor Graphics

nanometrics

Nikon

SEMATECH

TEL